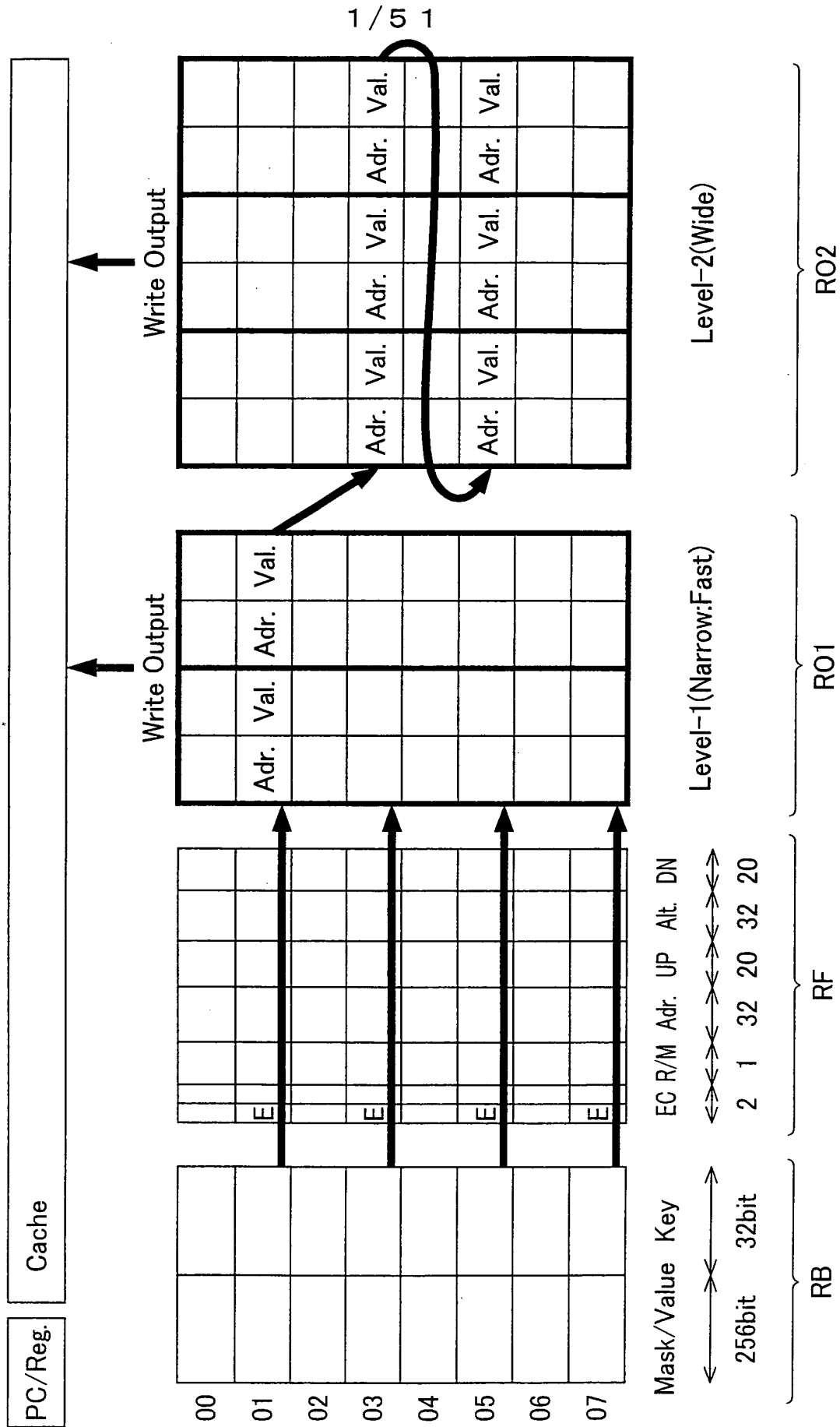


FIG. 1



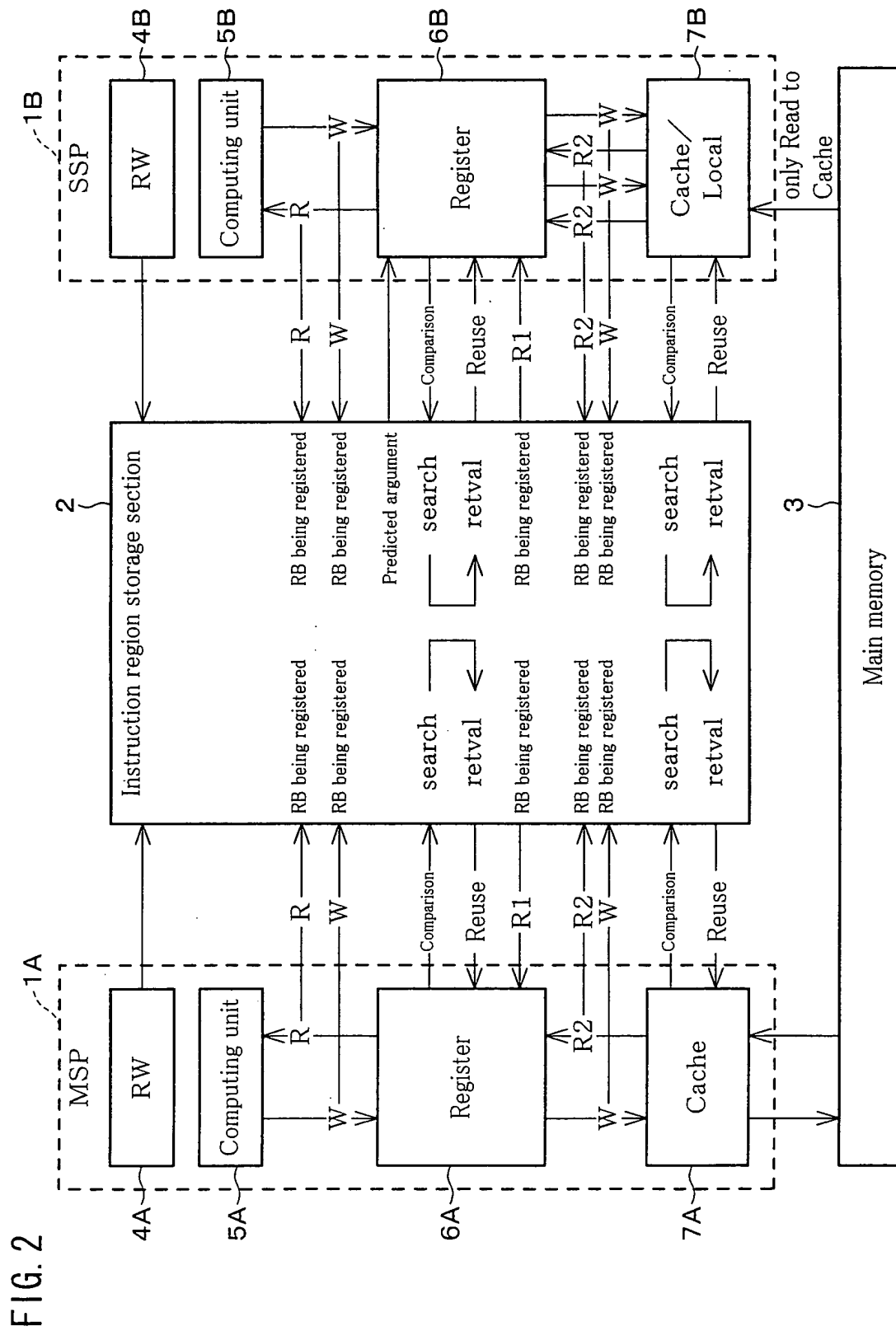


FIG. 3

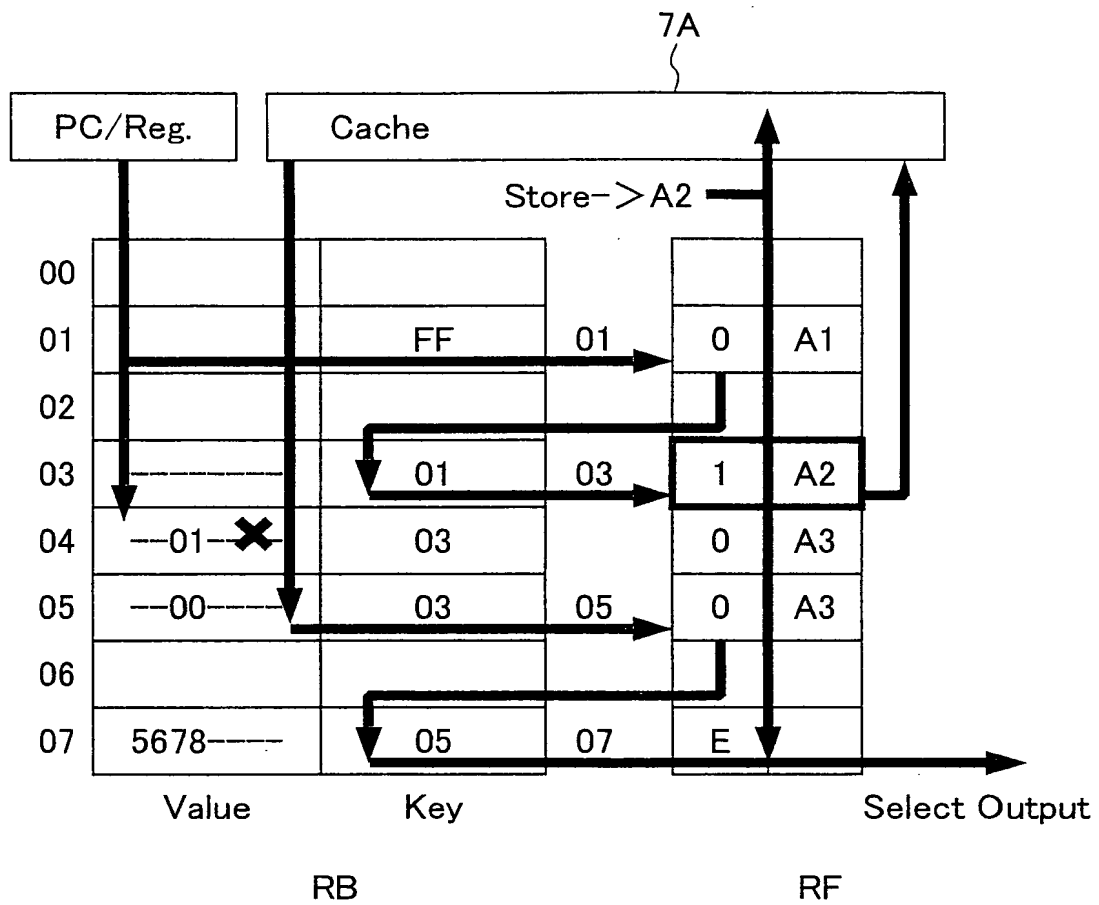


FIG. 4(a)

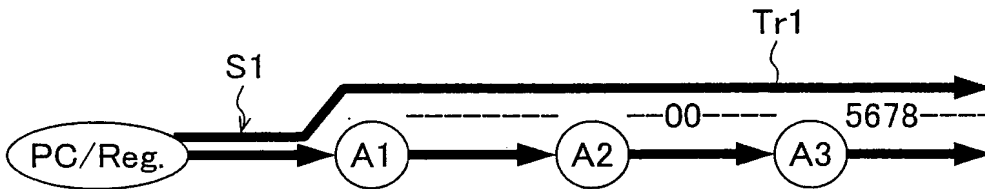


FIG. 4(b)

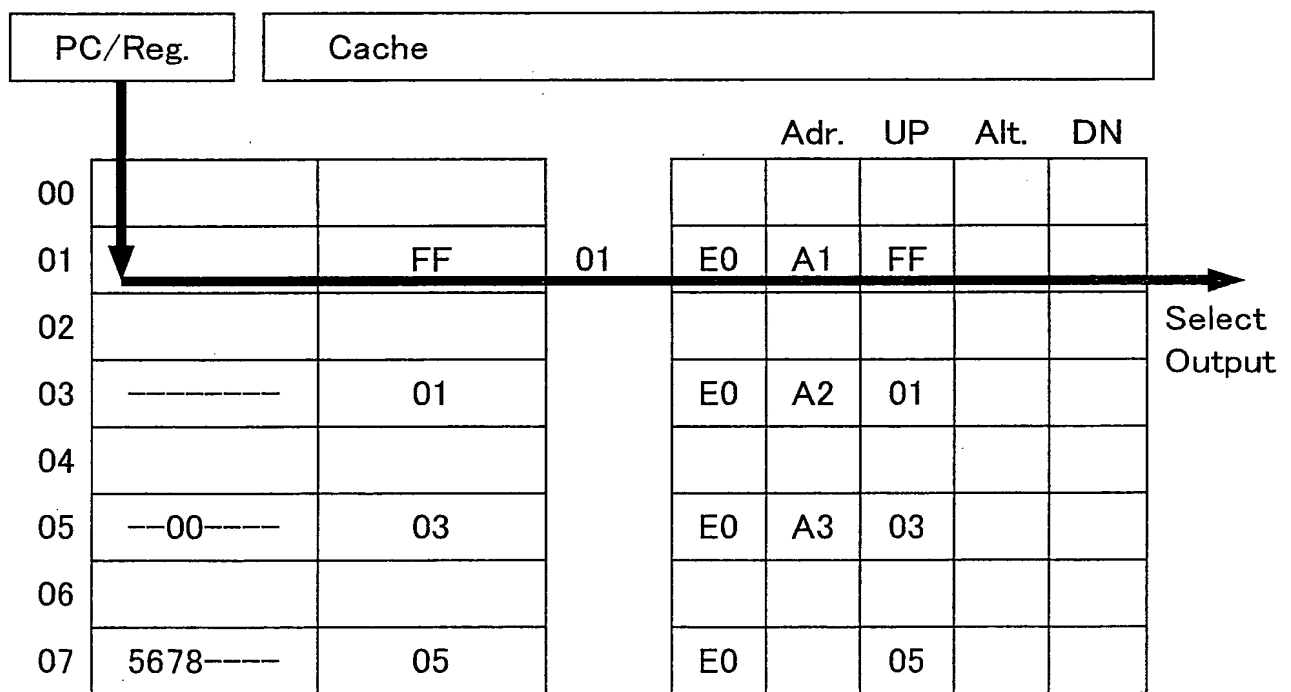


FIG. 5(a)

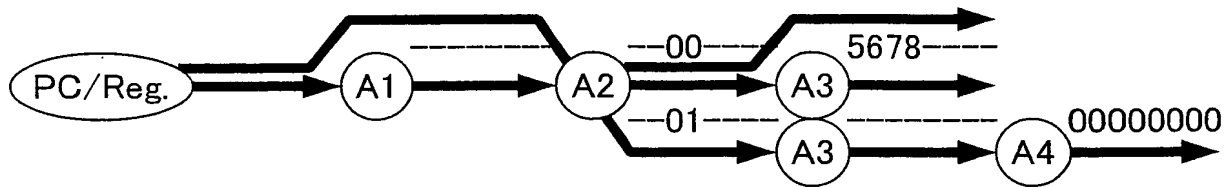


FIG. 5(b)

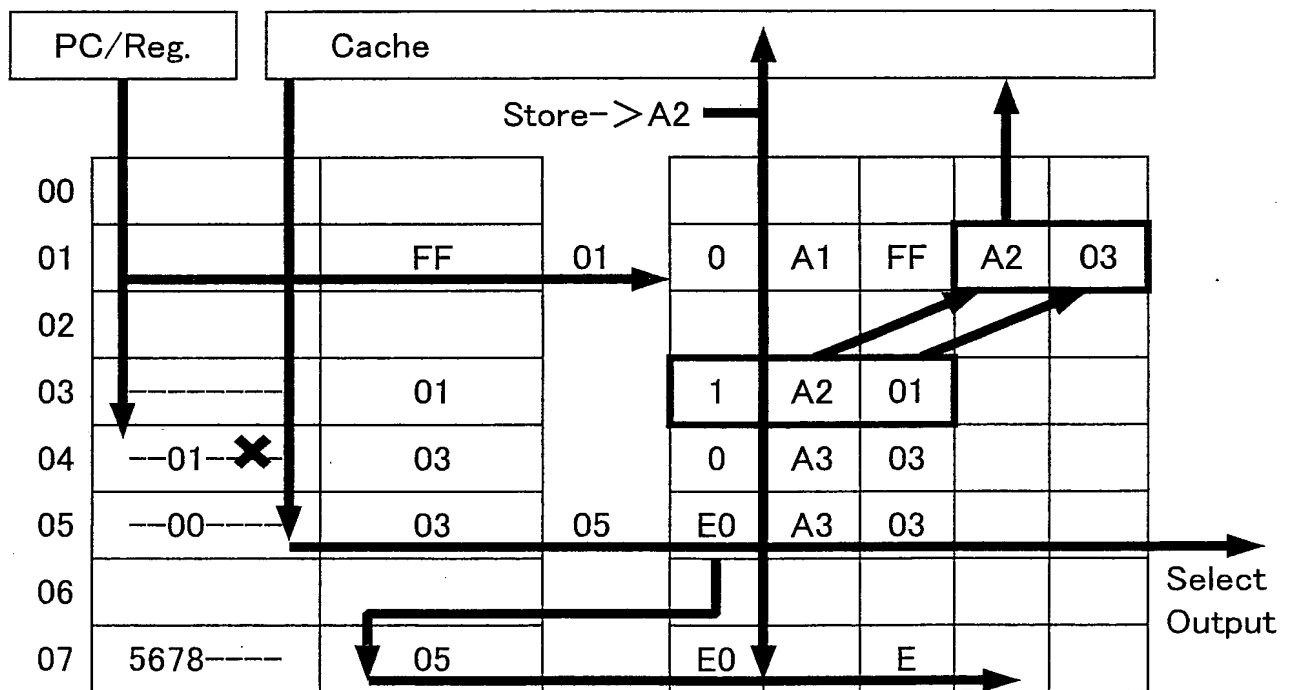


FIG. 6

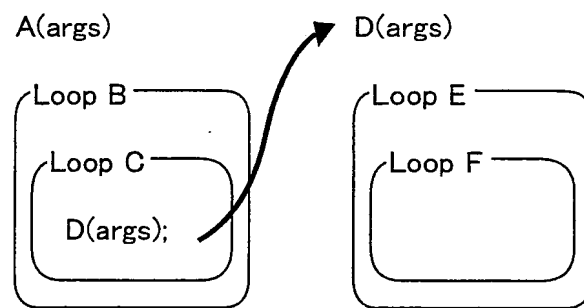


FIG. 7

Func. and Loop

Loop only

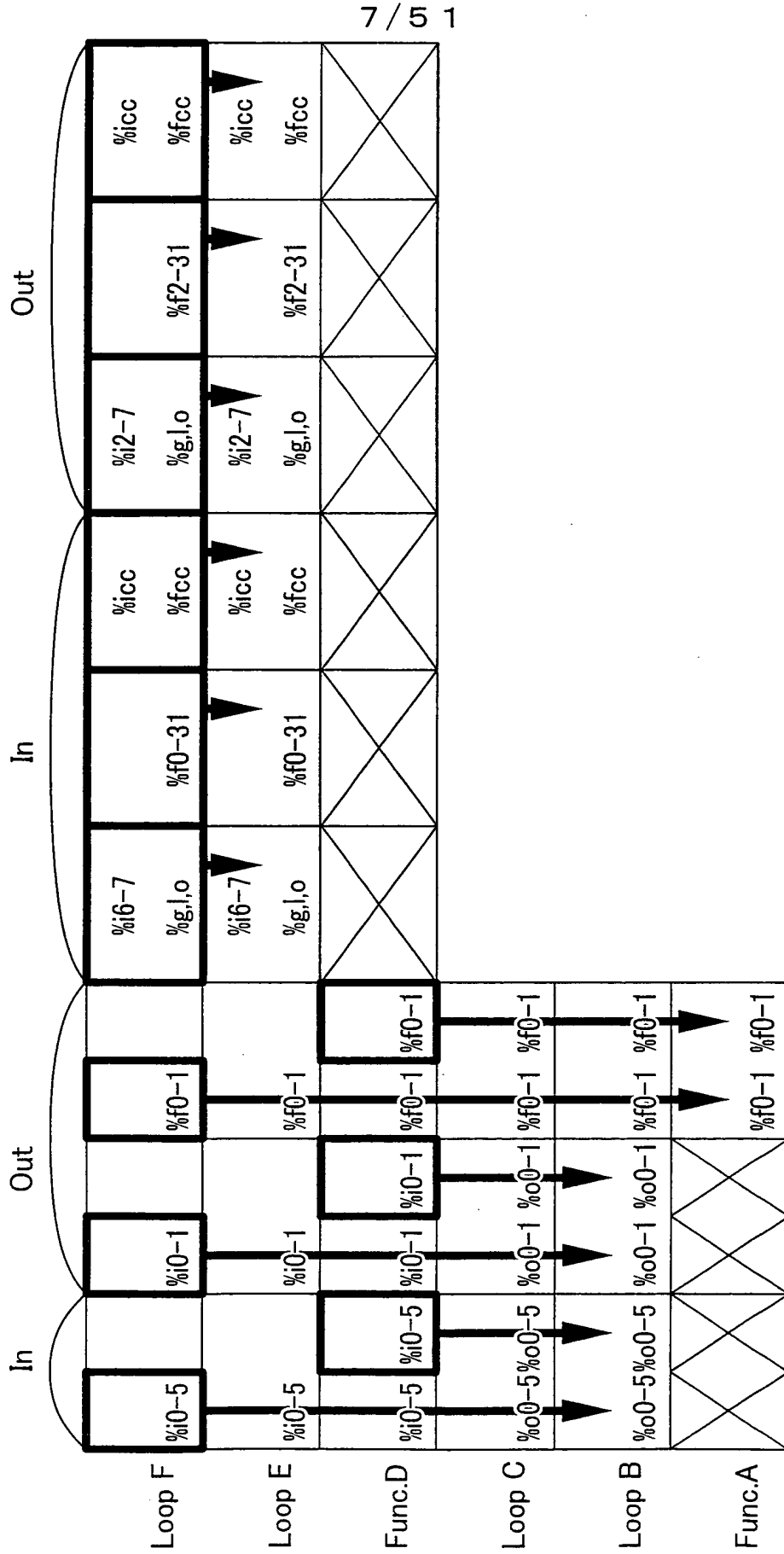


FIG. 8

(Pointer for Multilevel Memorization)

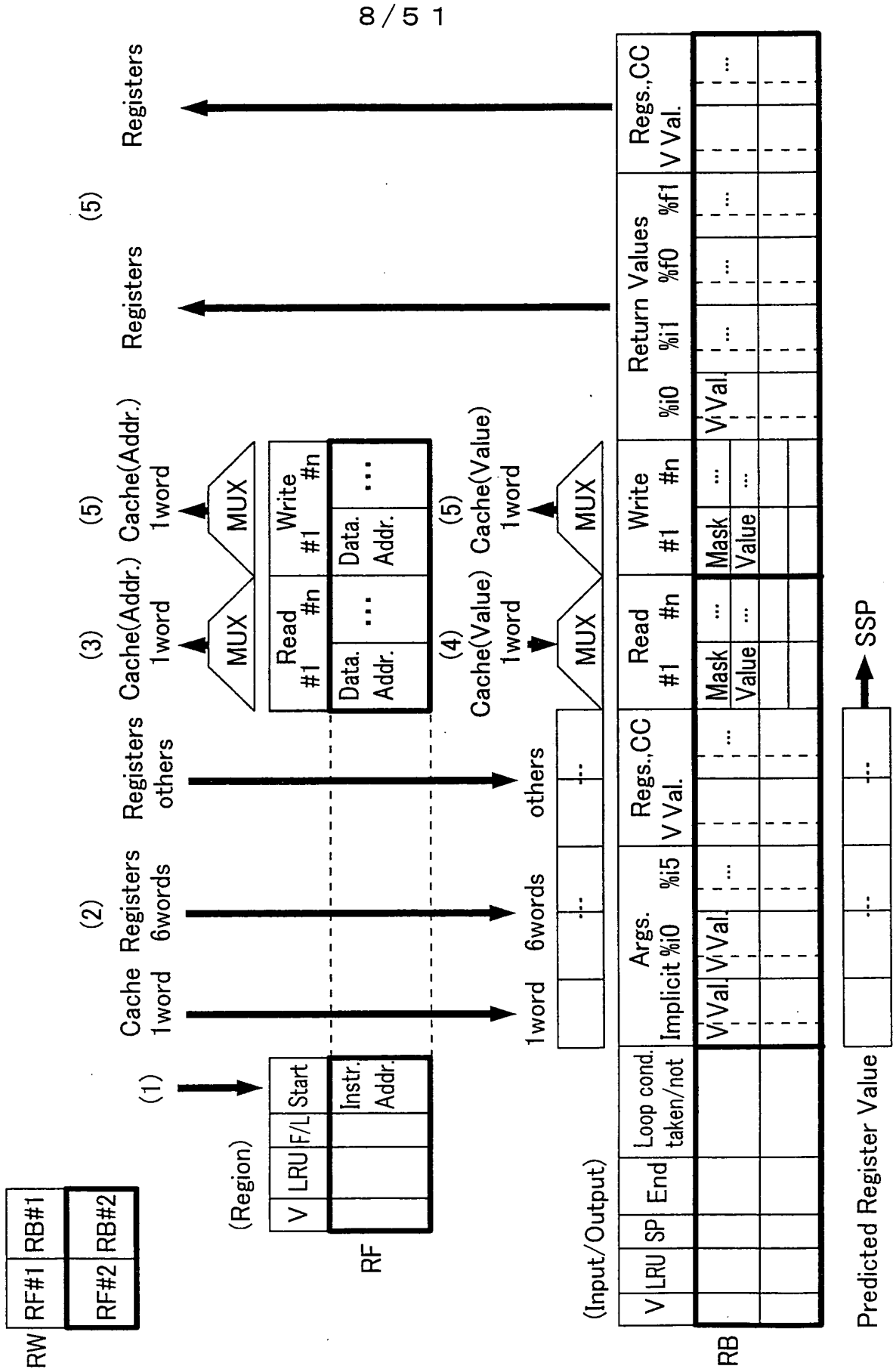


FIG. 9

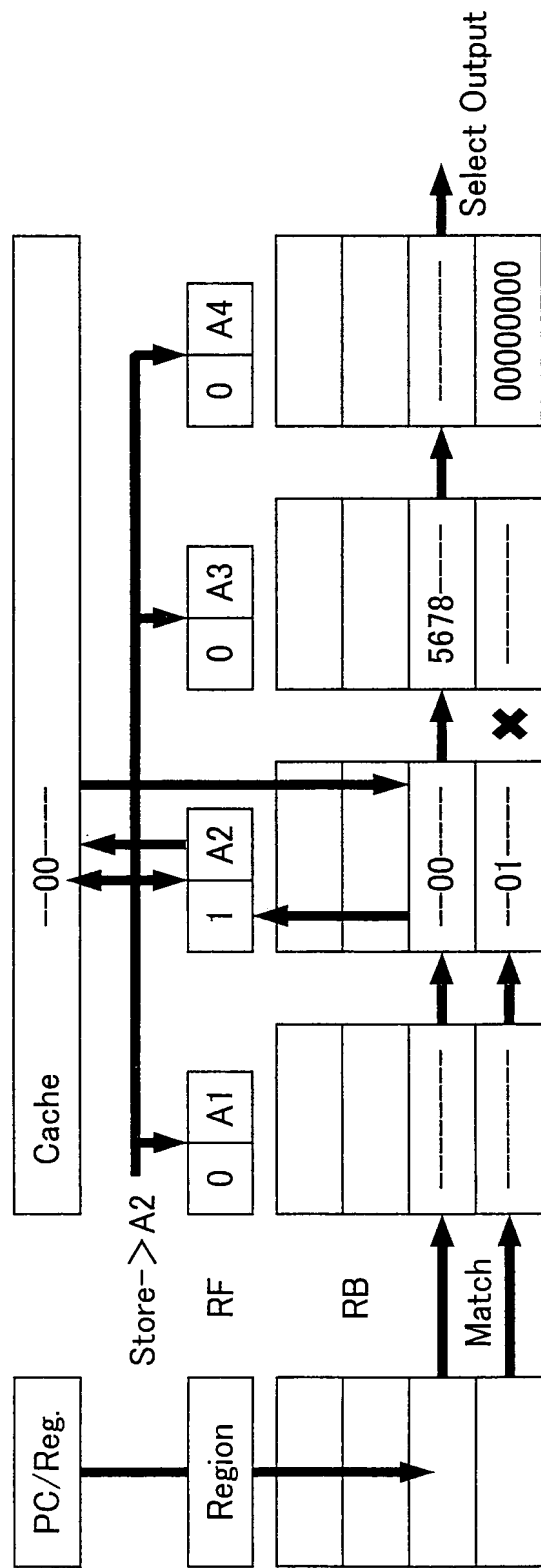


FIG. 10

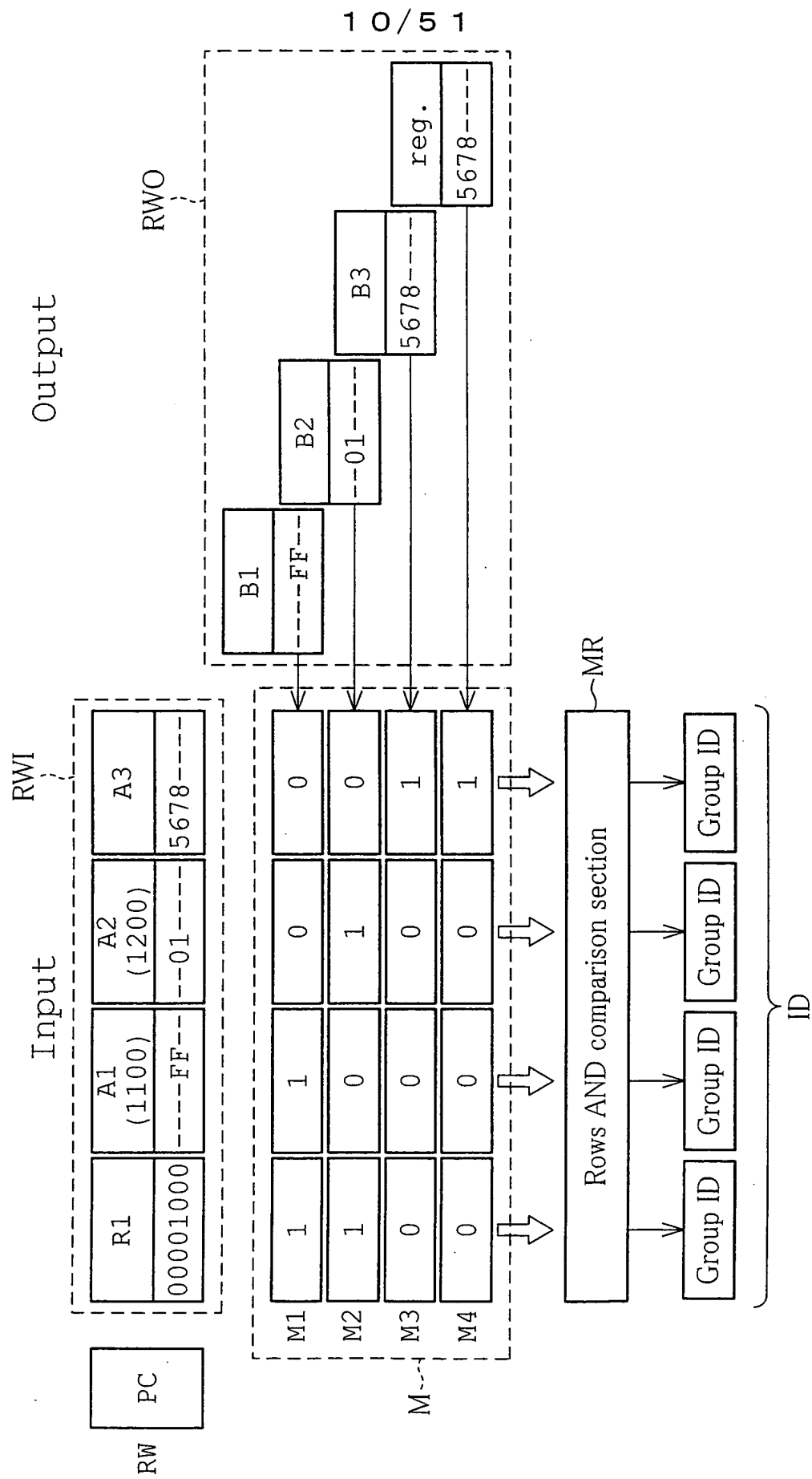


FIG. 11

```
PC:load  [R1+100] (----FF--)  -> reg.  
      store reg.              -> B1 (----FF--)  
      load  [R1+200] (--01----) -> reg.  
      store reg.              -> B2 (--01----)  
      load  A3(5678----)      -> reg.  
      store reg.              -> B3(5678----)
```

FIG. 12

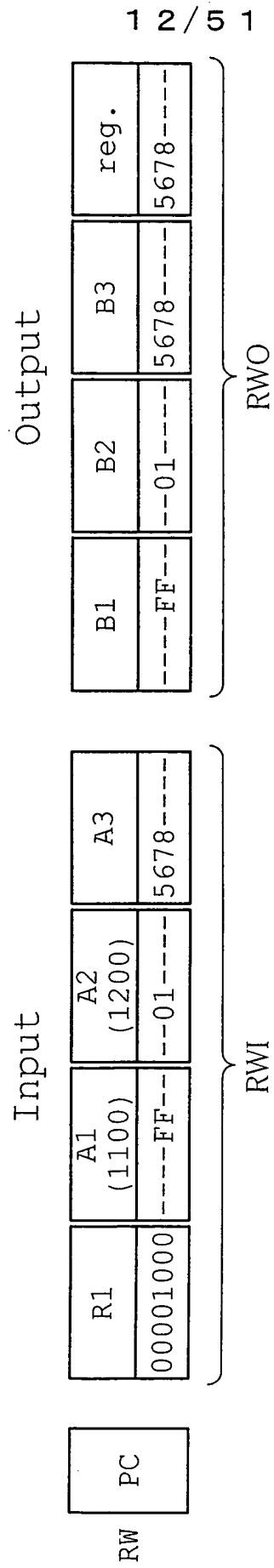


FIG. 13

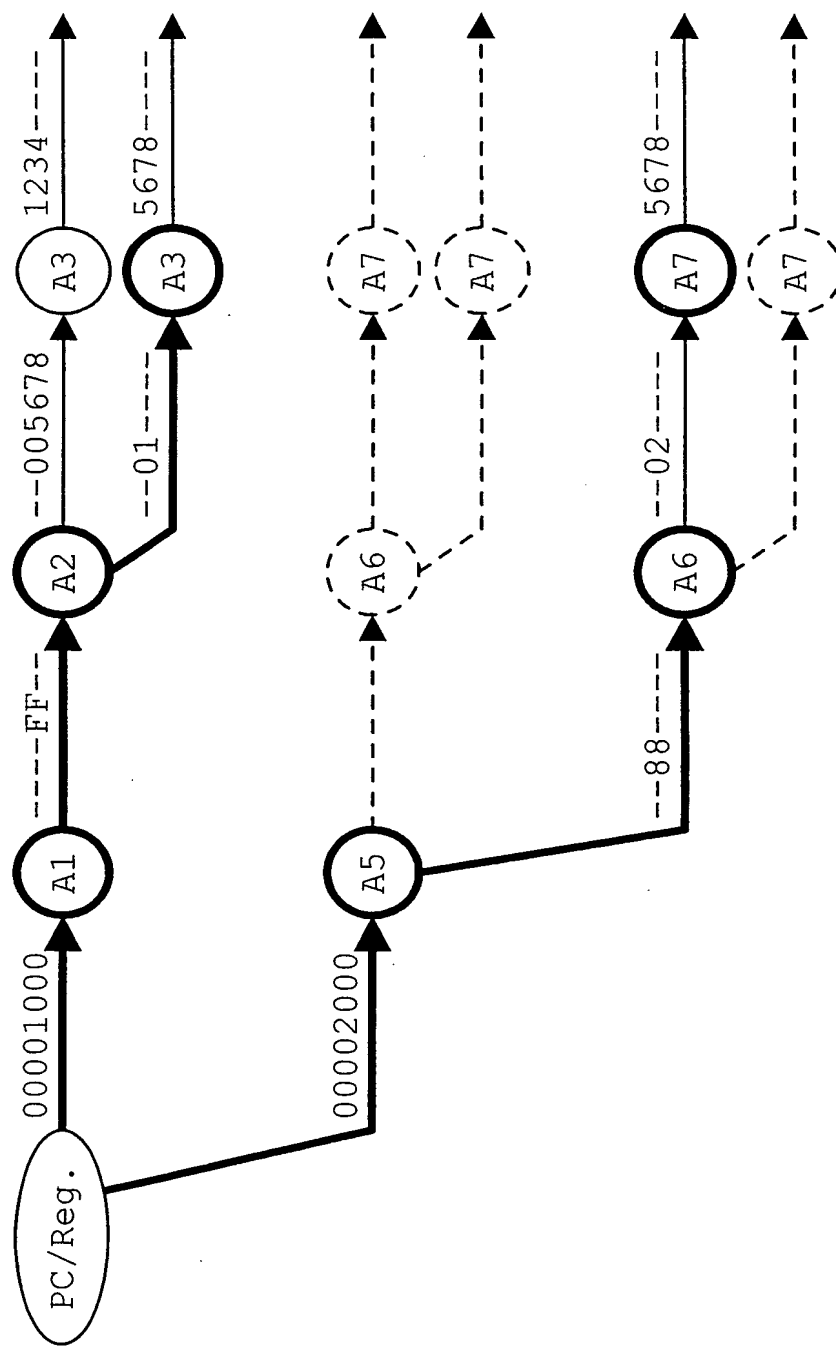


FIG. 14

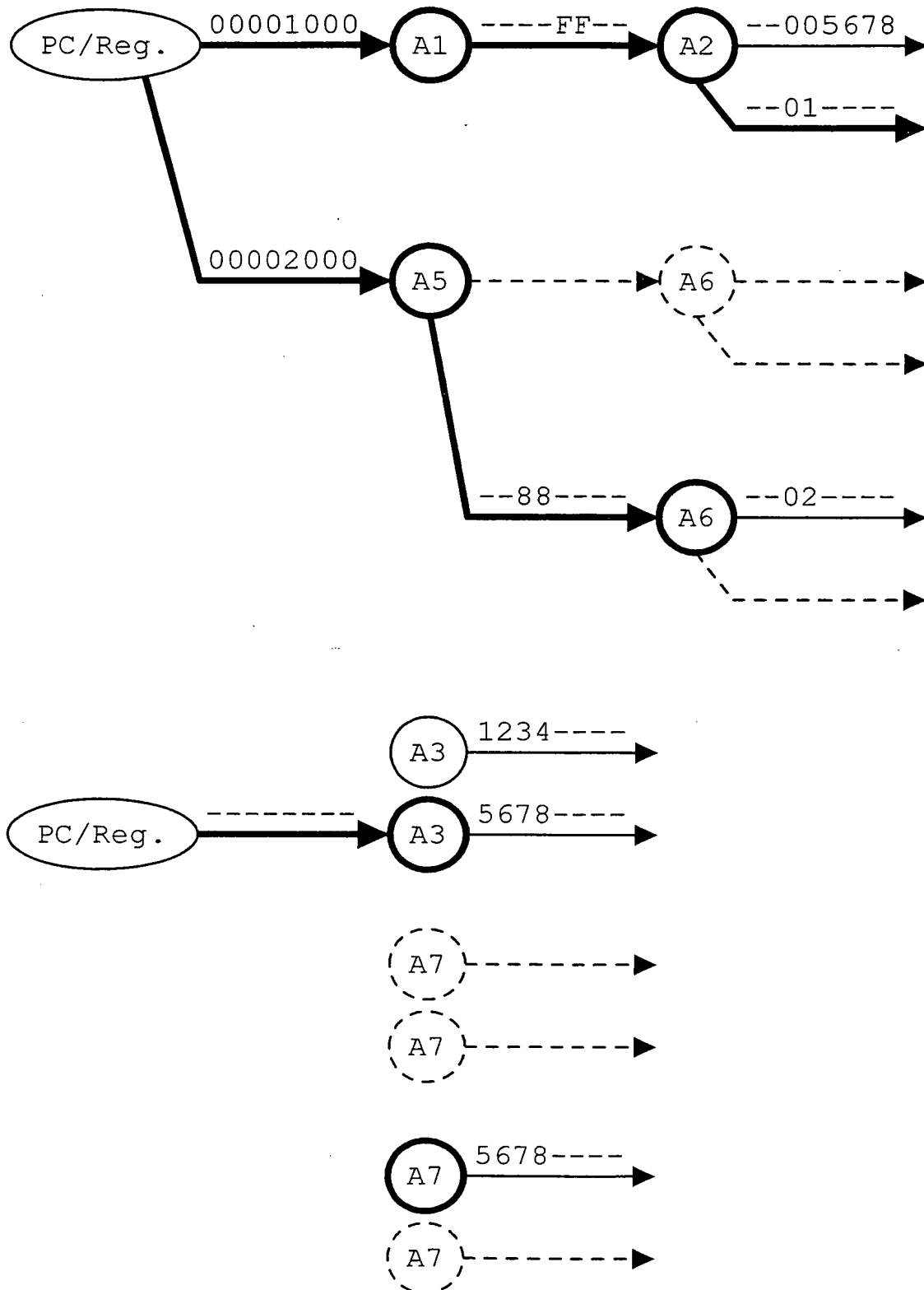


FIG. 15

PC: 1000

$\text{Id}(A1) \rightarrow R1$

$\text{Id}(A2) \rightarrow R2$

$\text{Id}(A2+R2) \rightarrow R2$

$\text{Id}(A3) \rightarrow R3$

$\text{Id}(A4=R1+R2) \rightarrow R4$

FIG. 16

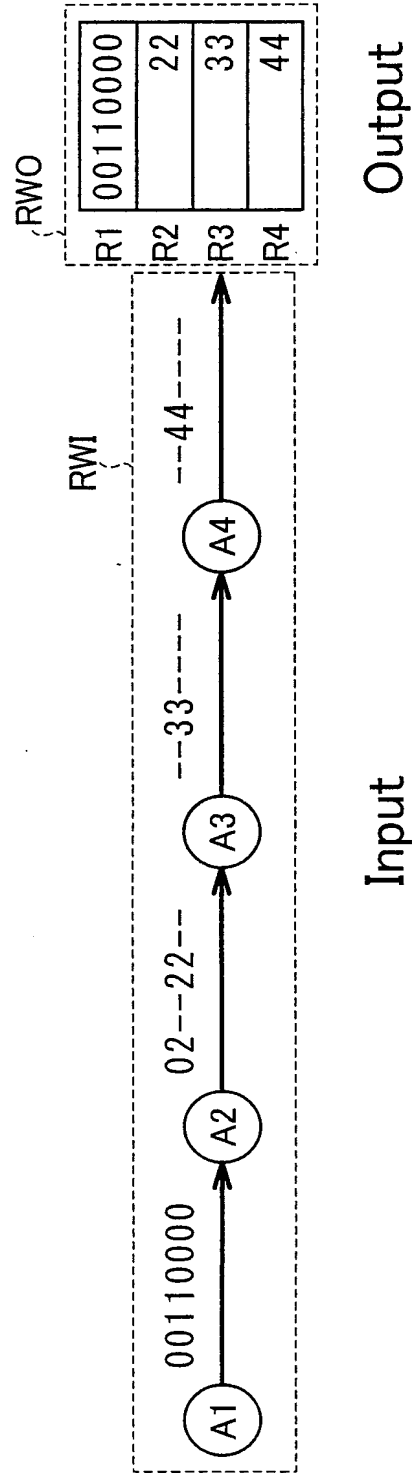


FIG. 17

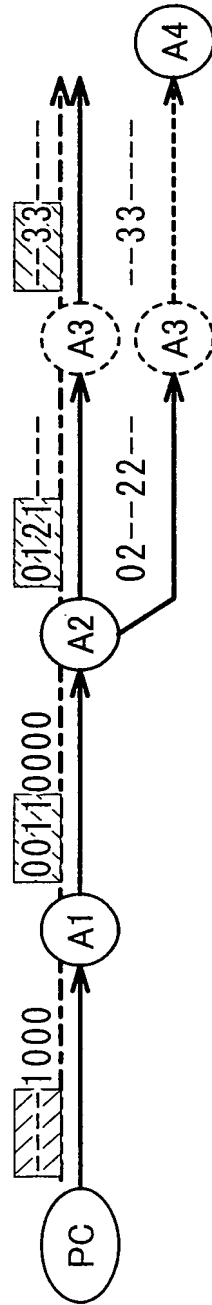


FIG. 18

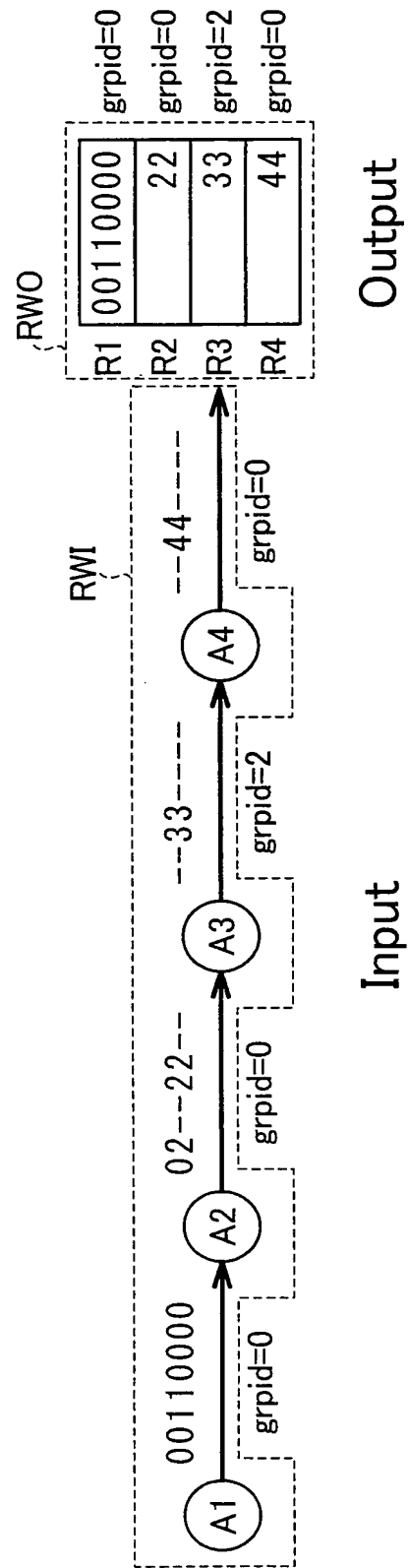


FIG. 19

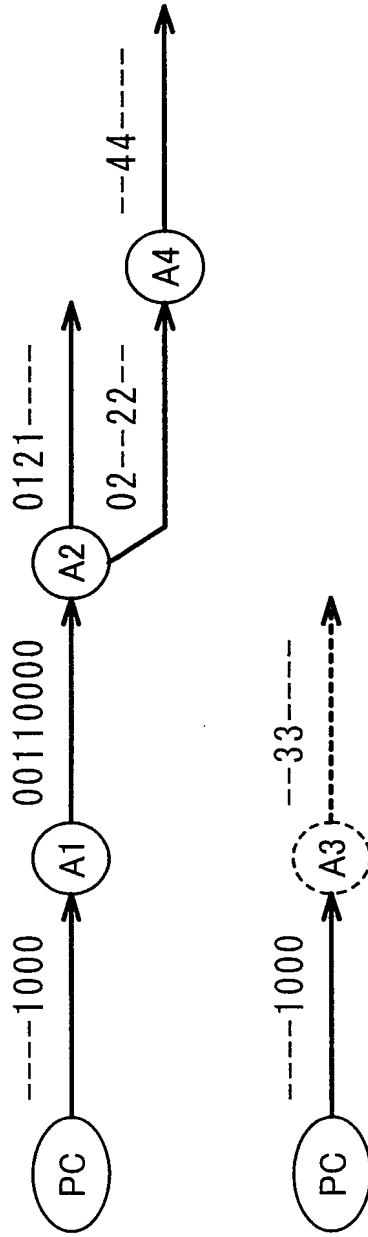


FIG. 20

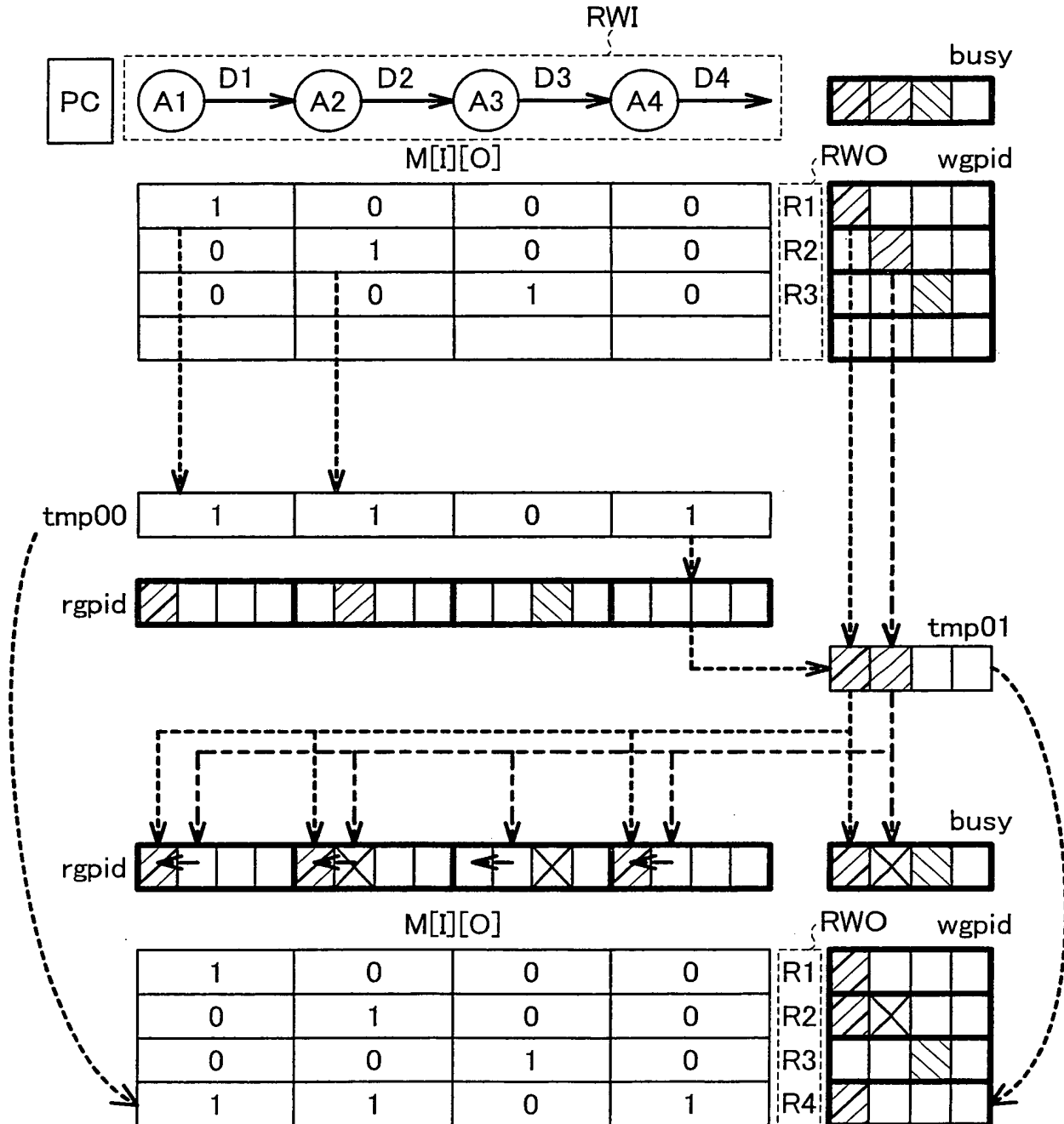


FIG. 21

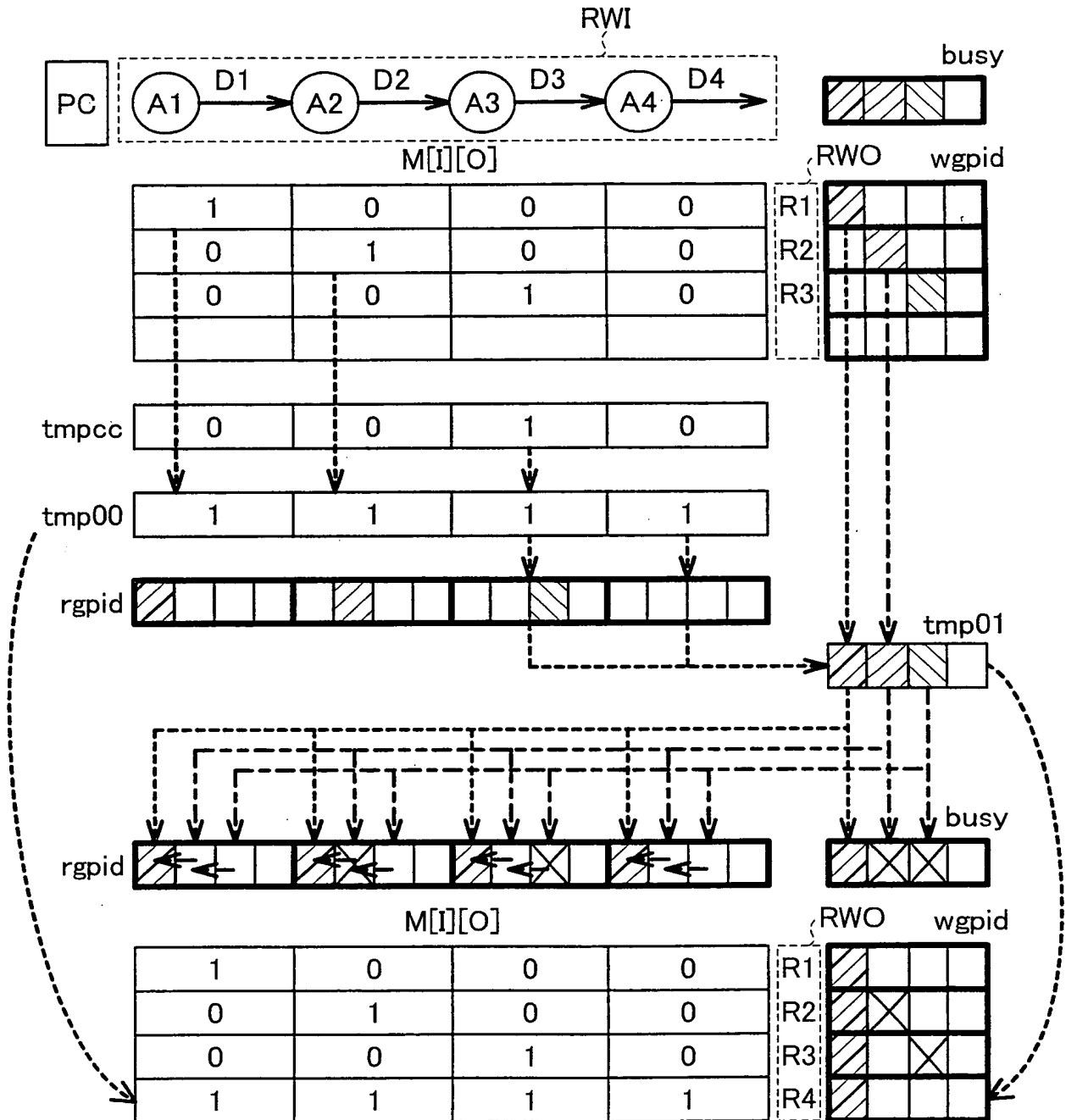


FIG. 22




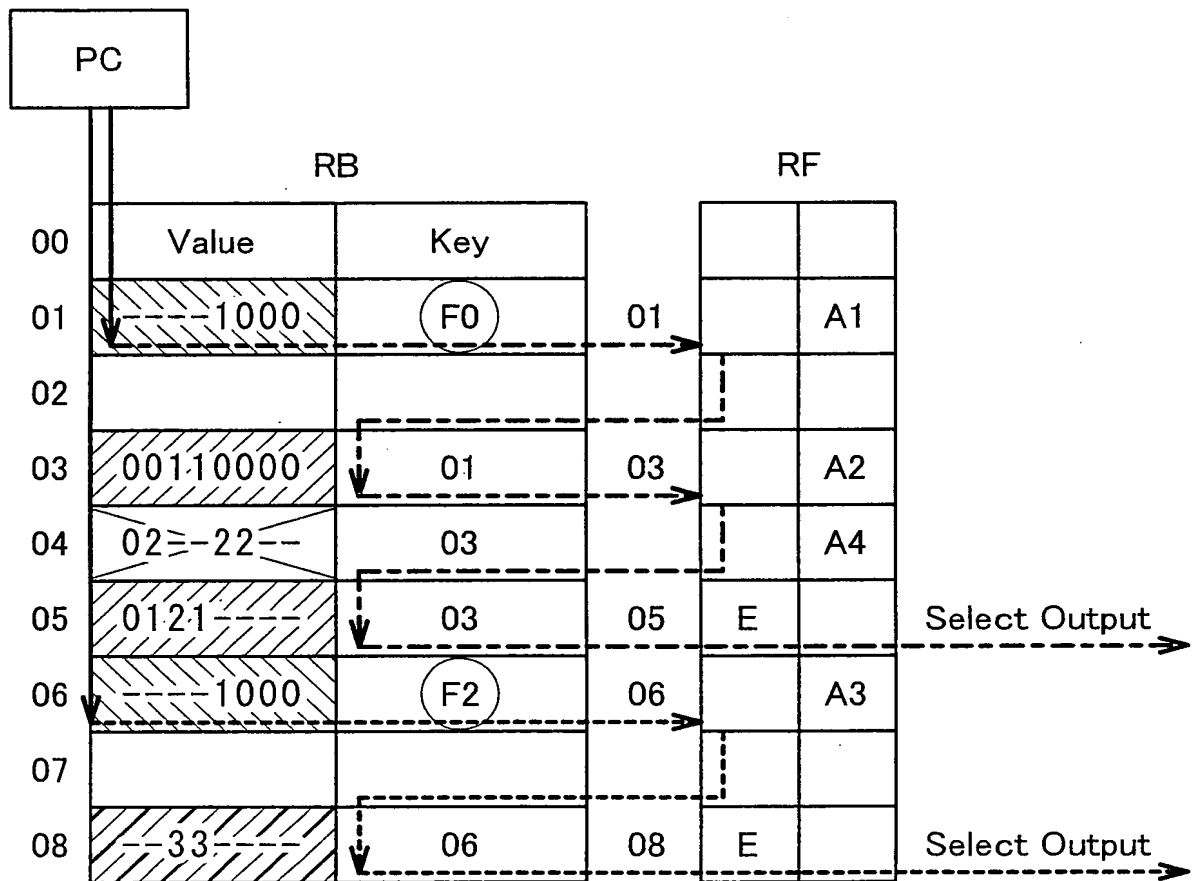
ld (A1) -> R1
ld (A2) -> R2
ld (A2+R2) -> R2
ld (A3) -> R3
subcc R3
bz xxxx
ld (=+) -> R4

FIG. 23



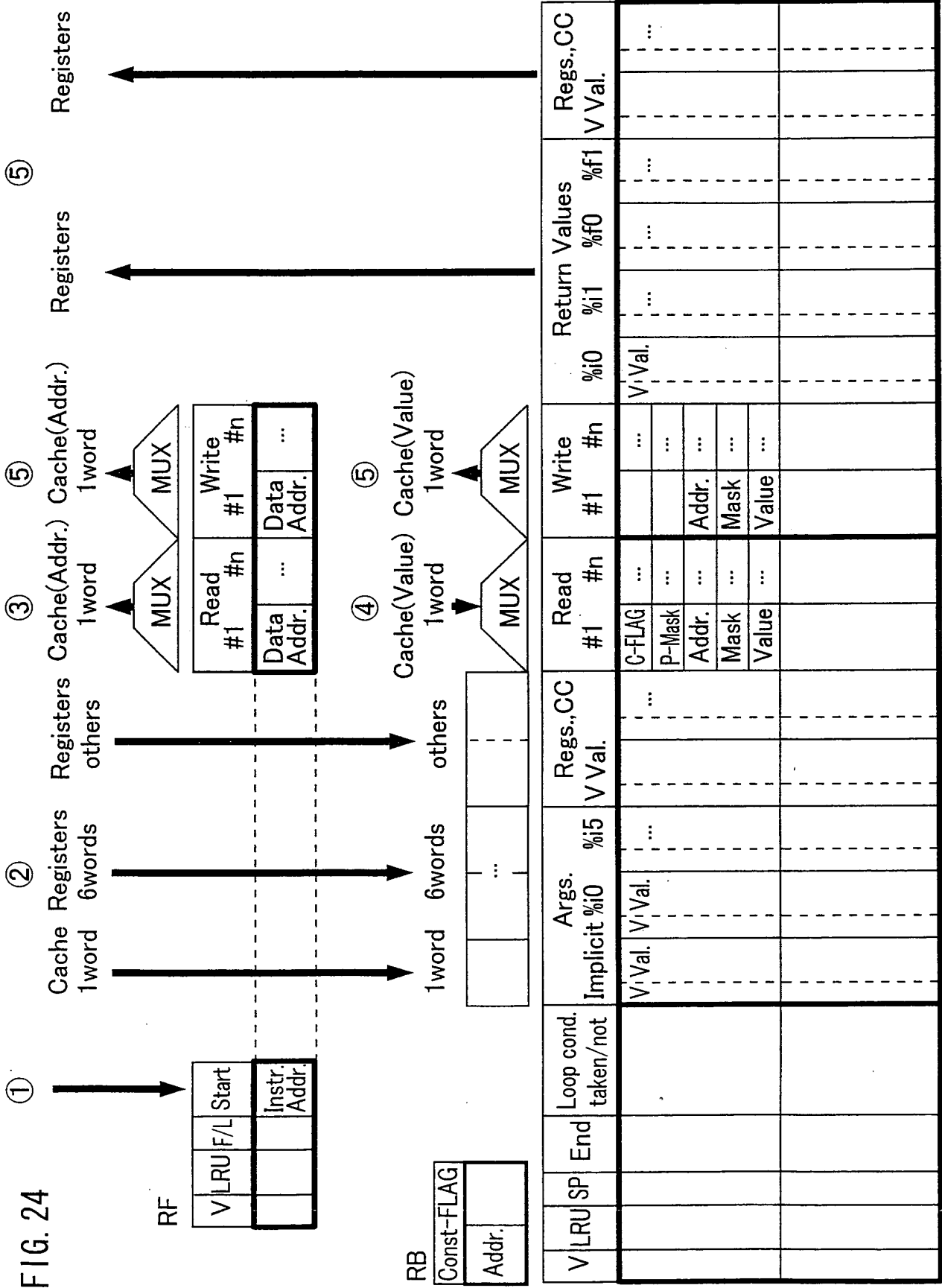


FIG. 25

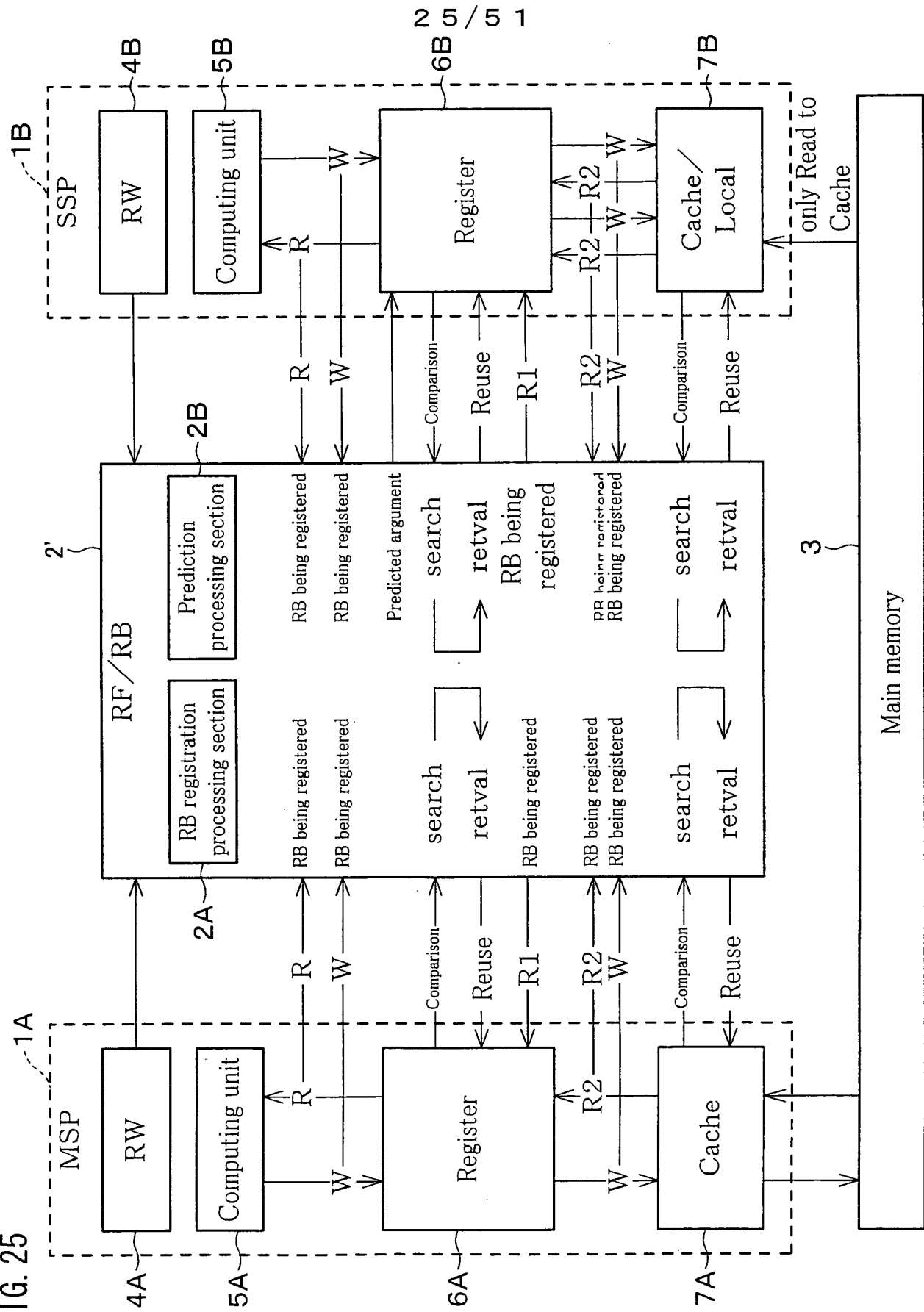


FIG. 26

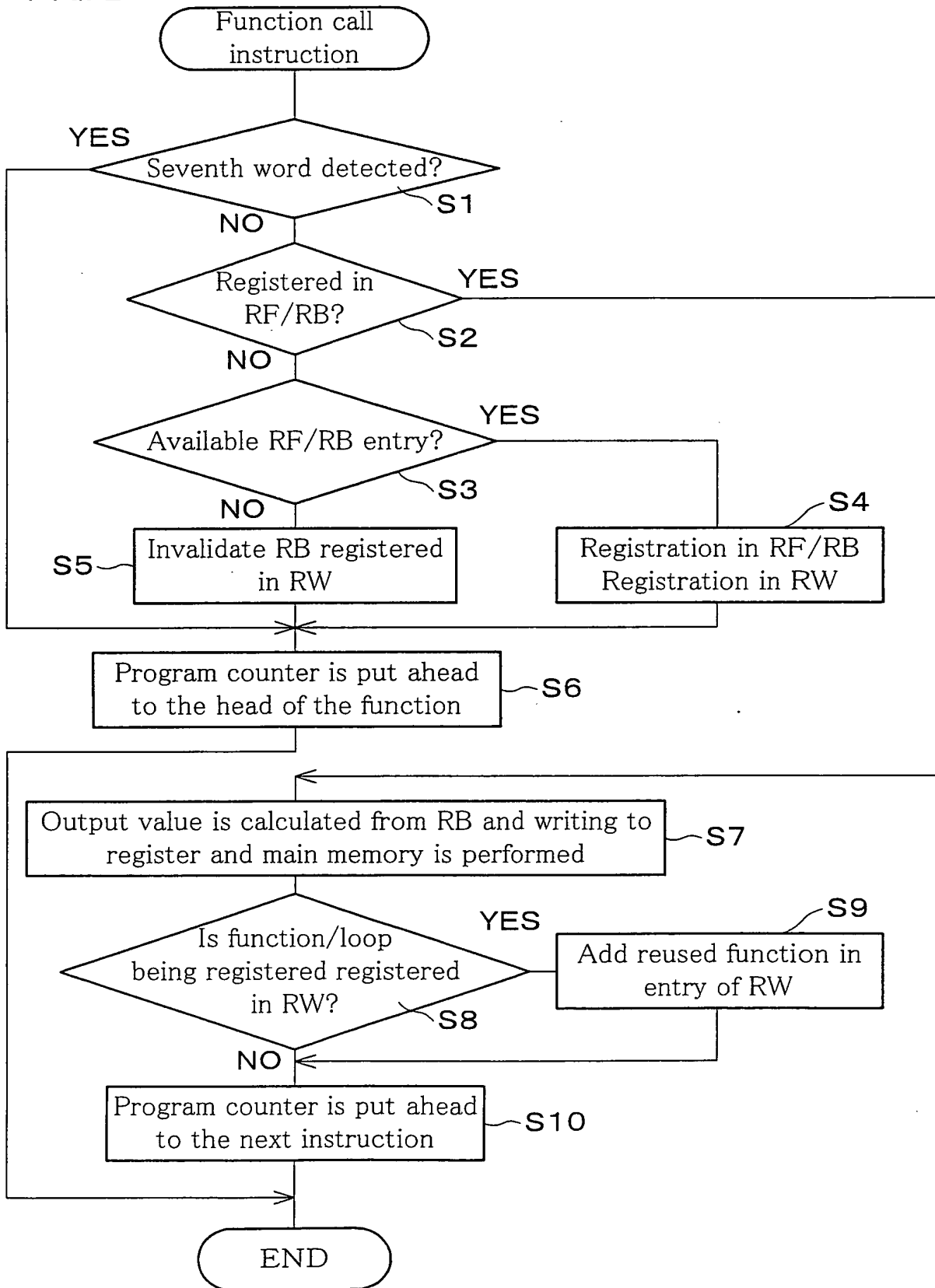


FIG. 27

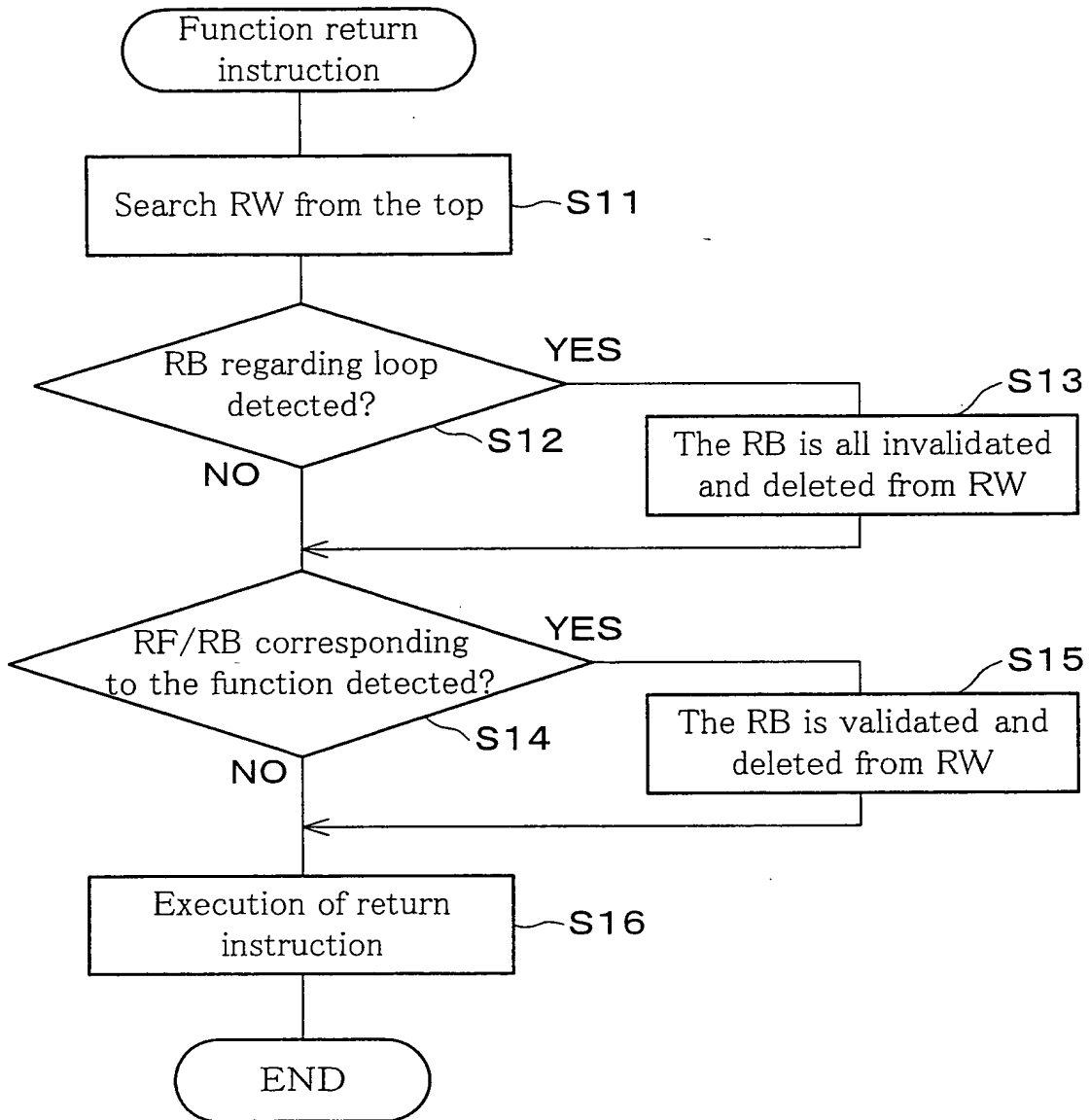


FIG. 28

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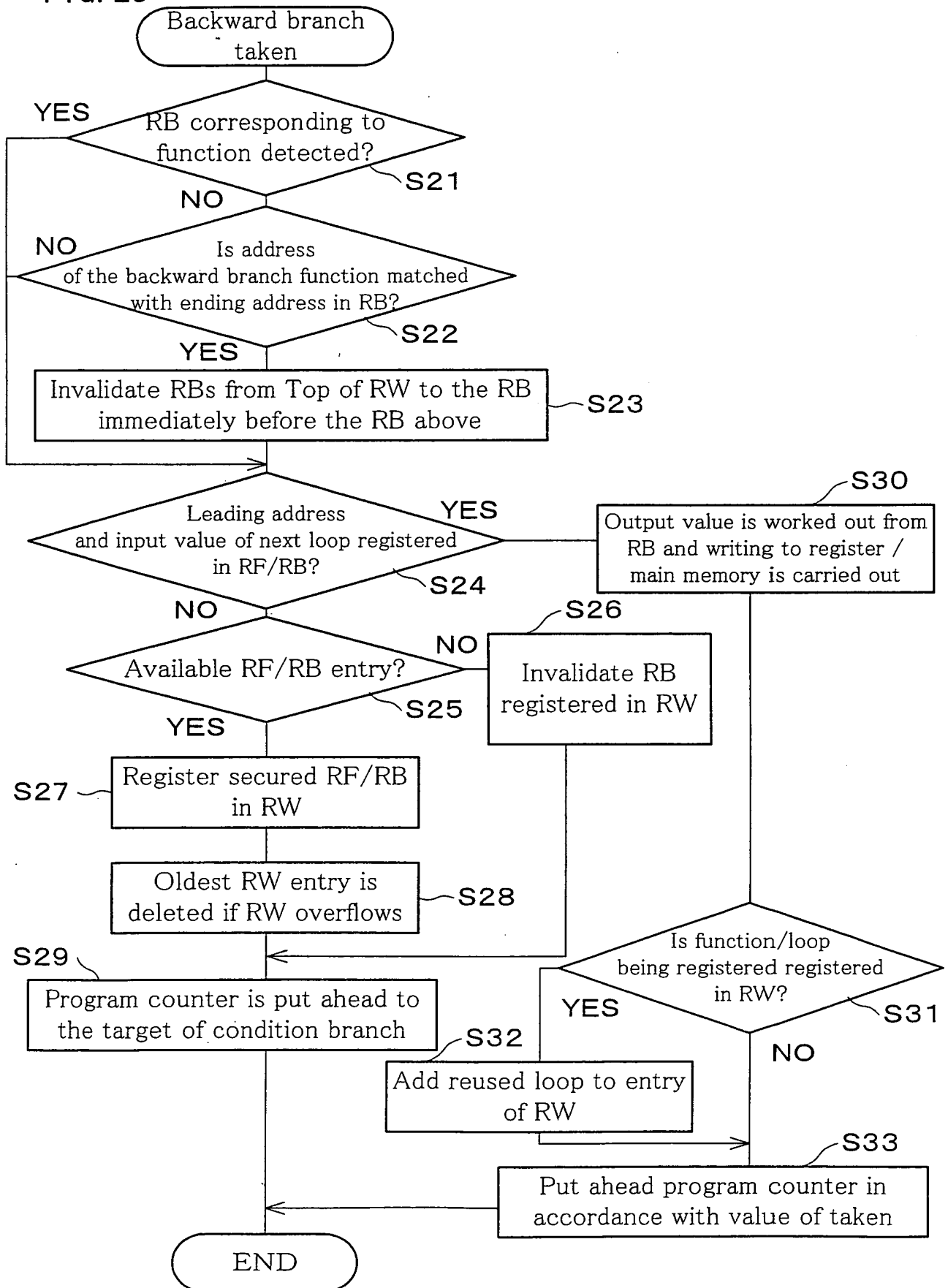


FIG. 29

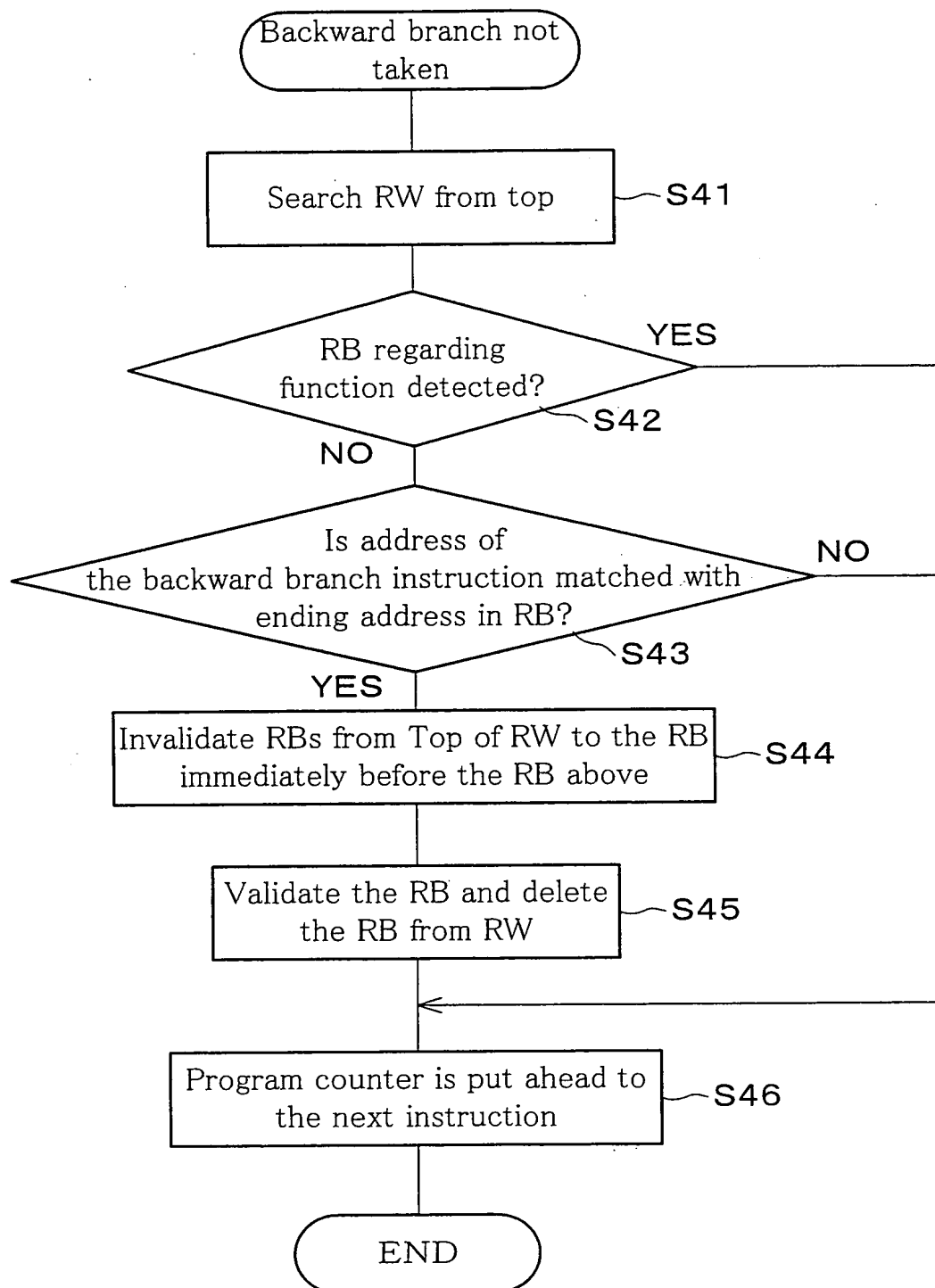


FIG. 30

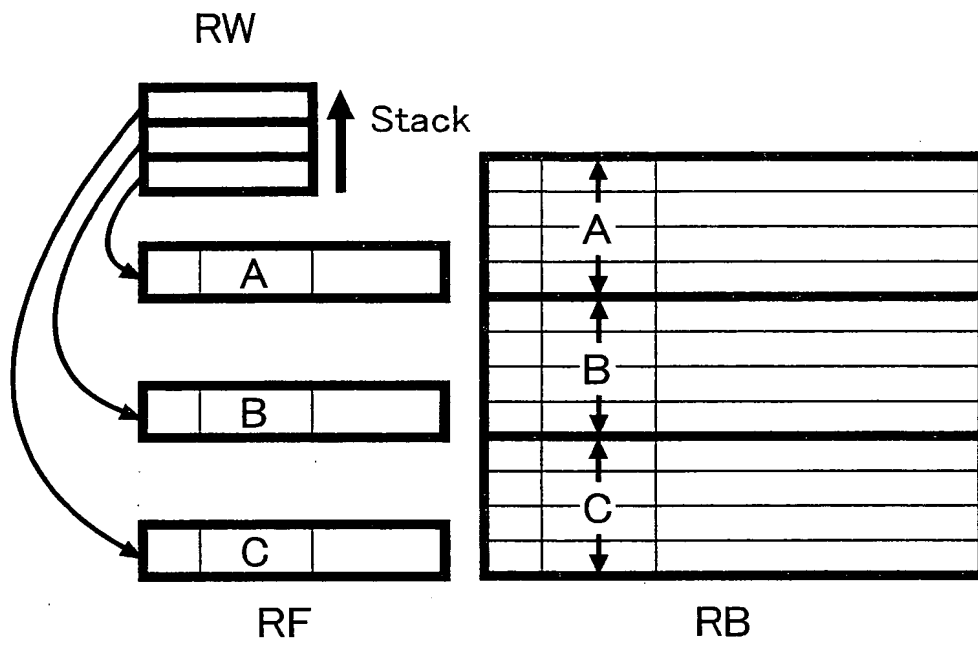


FIG. 31

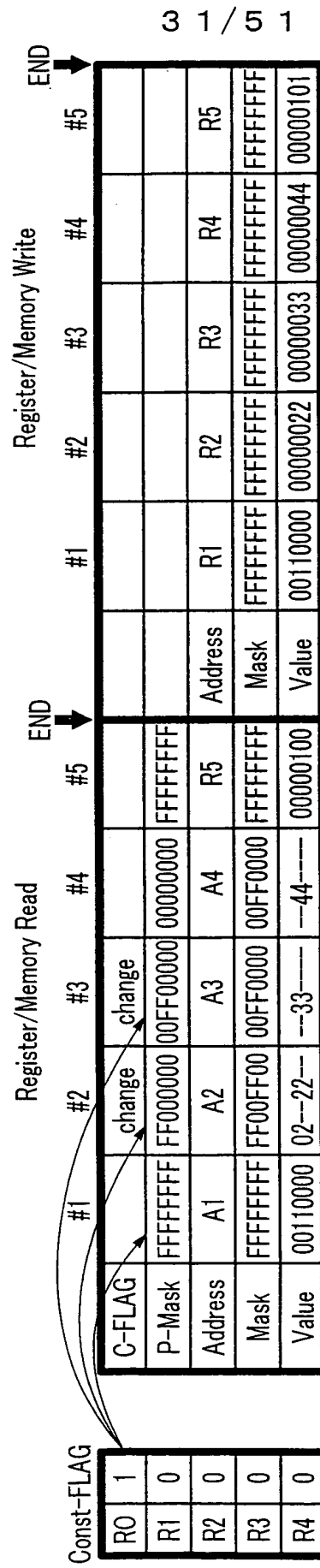


FIG. 32

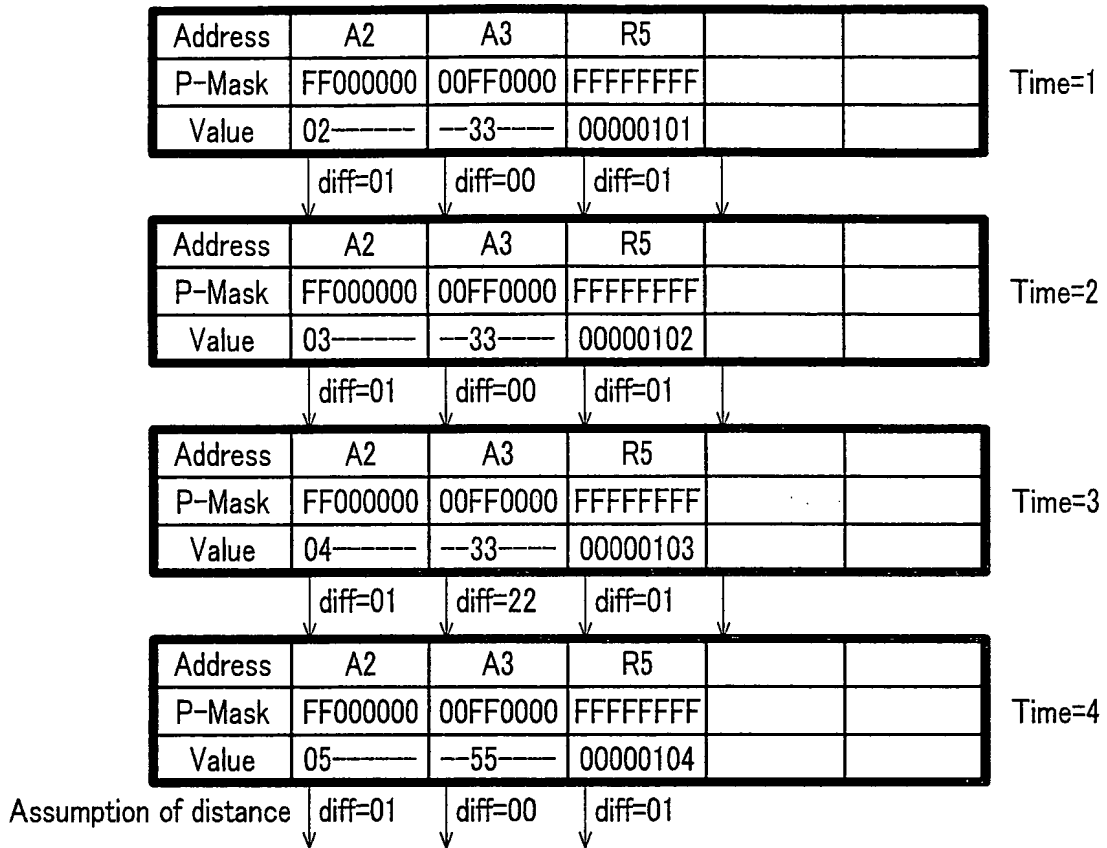


FIG. 33

Address	A2	R5	A2+4	A3	
Mask	FF000000	FFFFFFFF	0000FF00	00FF0000	
Value	06-----	00000105	-----26--	--55----	

Predicted distance=1

Address	A2	R5	A2+4	A3	
Mask	FF000000	FFFFFFFF	000000FF	00FF0000	
Value	07-----	00000106	-----27	--55----	

Predicted distance=2

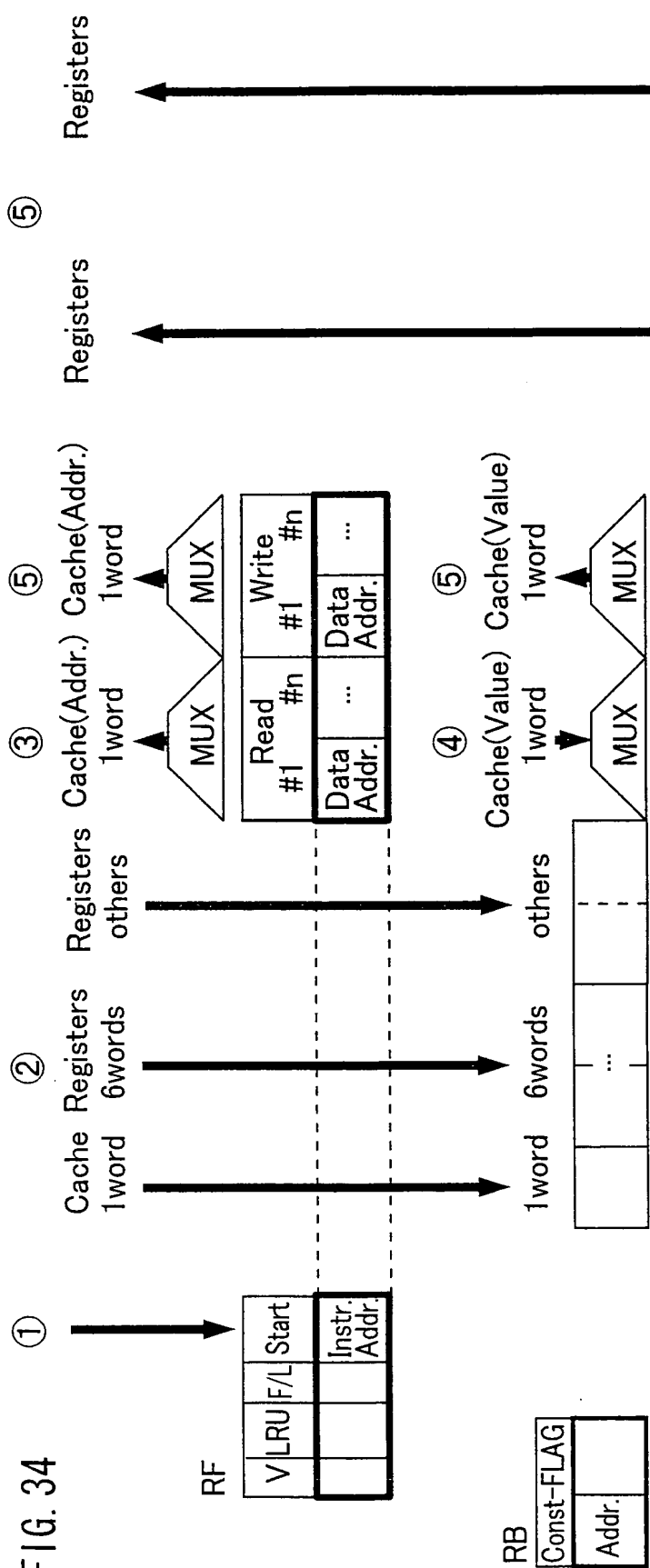
Address	A2	R5	A2+8	A3	
Mask	FF000000	FFFFFFFF	FF000000	00FF0000	
Value	08-----	00000107	28-----	--66----	

Predicted distance=3

Address	A2	R5	A2+8	A3	
Mask	FF000000	FFFFFFFF	00FF0000	00FF0000	
Value	09-----	00000108	--29----	--66----	

Predicted distance=4

FIG. 34



RB

Const-FLAG
Addr.

V LRU SP	End	Loop cond. taken/not	Args. Implicit %i0	Regs., CC V Val.	Read #1 #n	Write #1 #n	Return Values %i0 %i1 %f0 %f1	Regs., CC V Val.
			V'Val. V'Val.		C-FLAG		V'Val.	
					P-Mask			
					Addr.	Addr.		
					Mask	Mask		
					S-Count	S-Count		
					Value	Value		

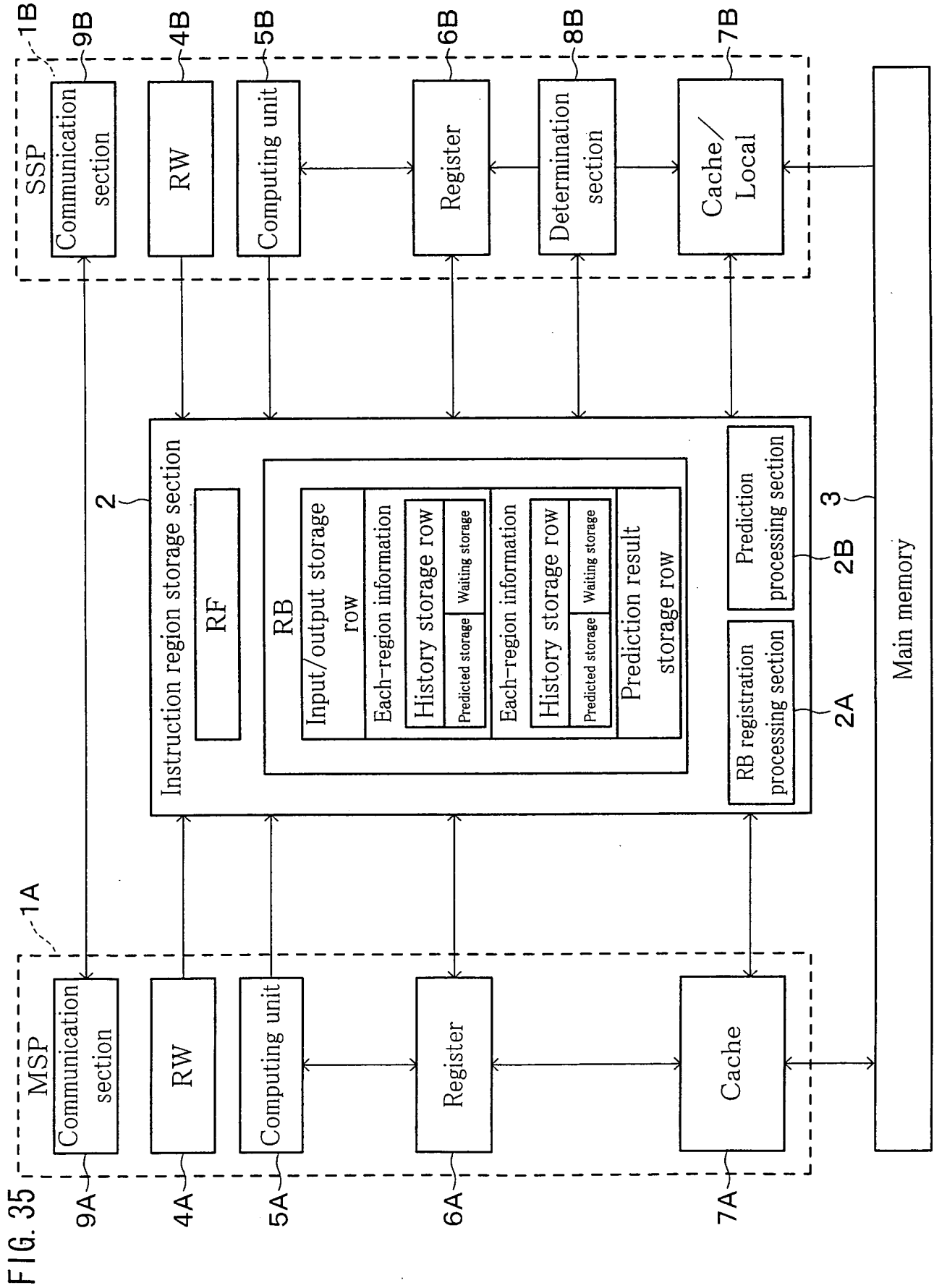
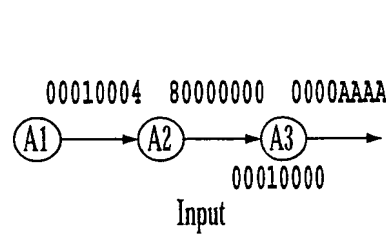


FIG. 36 (a)

```

loop:(PC=1000)
1: set A1 -> R1
2: ld (A1=R1) -> Rx ... (00010004)
3: set A2 -> R2
4: ld (A2=R2) -> Ry ... (80000000)
5: ld (A3=Rx-4) -> Rz ... (0000aaaa)
6: add Rx+4 -> Rx ... 00010008
7: st Rx -> (A1=R1) ... 00010008
8: shift Ry -> Ry ... 40000000
9: st Ry -> (A2=R2) ... 40000000
10: add Ry+Rz -> Rz ... 4000aaaa
11: st Rz -> (A4=Rx) ... 4000aaaa
12: br loop
    
```

FIG. 36 (b)



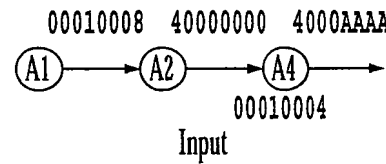
Rx	00010008
Ry	40000000
Rz	4000AAAA
A1	00010008
A2	40000000
A4 (00010004)	4000AAAA

FIG. 36 (c)

```

loop:(PC=1000)
set A1 -> R1
ld (A1=R1) -> Rx ... (00010008)
set A2 -> R2
ld (A2=R2) -> Ry ... (40000000)
ld (A4=Rx-4) -> Rz ... (4000aaaa)
add Rx+4 -> Rx ... 0001000c
st Rx -> (A1=R1) ... 0001000c
shift Ry -> Ry ... 20000000
st Ry -> (A2=R2) ... 20000000
add Ry+Rz -> Rz ... 6000aaaa
st Rz -> (A5=Rx) ... 6000aaaa
br loop
    
```

FIG. 36 (d)



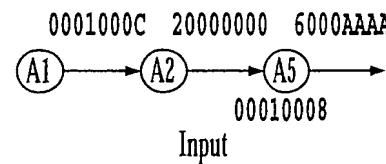
Rx	0001000C
Ry	20000000
Rz	6000AAAA
A1	0001000C
A2	20000000
A5 (00010008)	6000AAAA

FIG. 36 (e)

```

loop:(PC=1000)
set A1 -> R1
ld (A1=R1) -> Rx ... (0001000c)
set A2 -> R2
ld (A2=R2) -> Ry ... (20000000)
ld (A5=Rx-4) -> Rz ... (6000aaaa)
add Rx+4 -> Rx ... 00010010
st Rx -> (A1=R1) ... 00010010
shift Ry -> Ry ... 10000000
st Ry -> (A2=R2) ... 10000000
add Ry+Rz -> Rz ... 7000aaaa
st Rz -> (A6=Rx) ... 7000aaaa
br loop
    
```

FIG. 36 (f)



Rx	00010010
Ry	10000000
Rz	7000AAAA
A1	00010010
A2	10000000
A6 (0001000C)	7000AAAA

FIG. 37

Const-FLAG		Register/Memory Read				Register/Memory Write						
		#1	#2	#3	#1	#2	#3	#4	#5	#6		
R1	1	C-FLAG	change	change								
R2	1	P-Mask	FFFFFFFF	FFFFFFFF	00000000							
Rx	0	Address	A1	A2	A3	Address	Rx	Ry	Rz	A1	A2	A4
Ry	0	Mask	FFFFFFFF	FFFFFFFF	FFFFFFFF	Mask	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF
Rz	0	Value	00010004	80000000	0000AAAA	Value	00010008	40000000	4000AAAA	00010008	40000000	4000AAAA

3 7 / 5 1

FIG. 38(a)

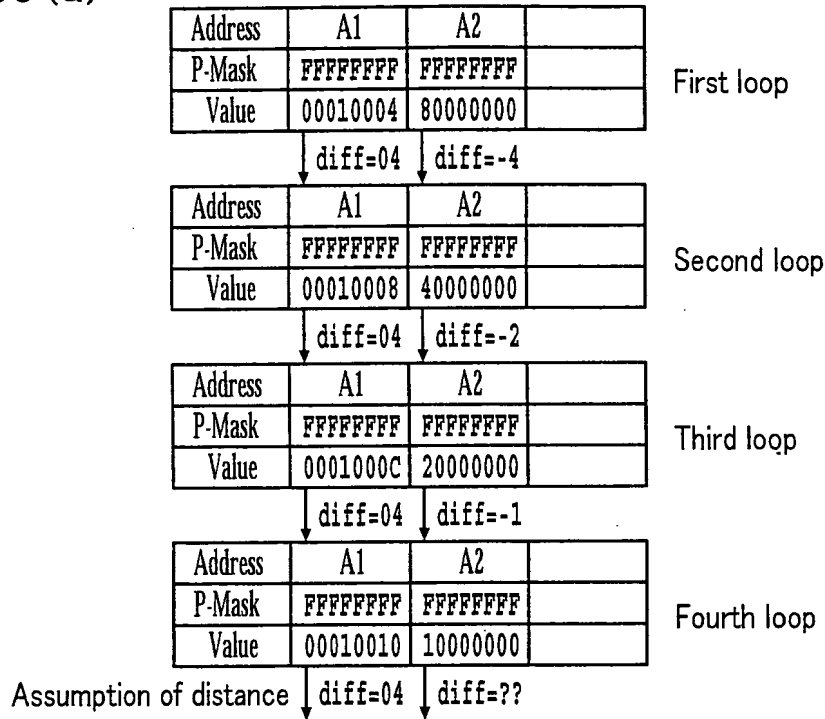


FIG. 38(b)

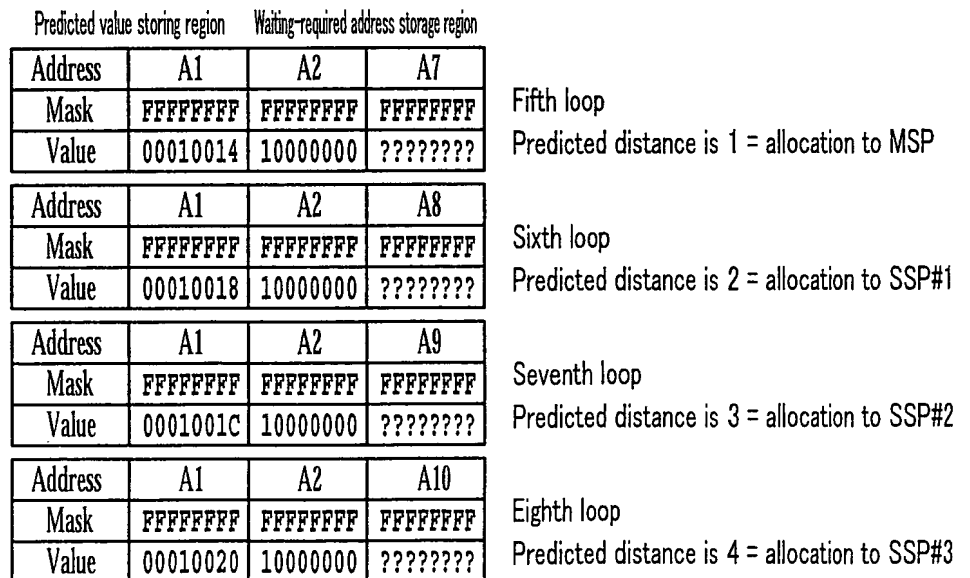


FIG. 39

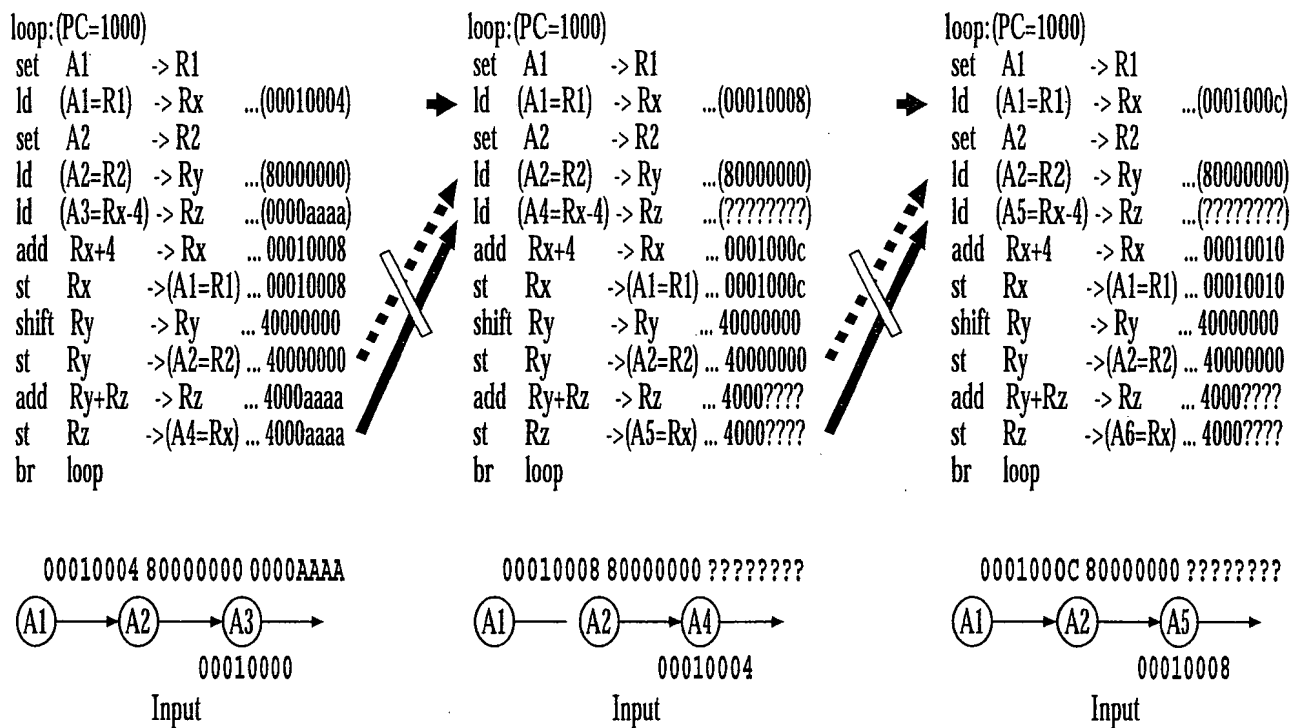


FIG. 40(a)

Register/Memory Read				Register/Memory Write					
	#1	#2	#3	#1	#2	#3	#4	#5	#6
C-FLAG	change	change							
P-Mask	FFFFFFFF	FFFFFFFF	00000000	Address	Rx	Ry	A1	A2	A4
Address	A1	A2	A3	Mask	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF
Mask	FFFFFFFF	FFFFFFFF	FFFFFFFF	S-Count			0001	0001	0001
Value	00010004	80000000	0000AAAA	Value	00010008	40000000	00010008	40000000	4000AAAA

FIG. 40(b)

				First loop			
Address	A1	A2	A3	Address	A1	A2	A4
P-Mask	FFFFFFFF	FFFFFFFF	00000000	Mask	FFFFFFFF	FFFFFFFF	FFFFFFFF
S-Count	0001	0001	0001	S-Count	0001	0001	0001
Value	00010004	80000000					
				Second loop			
Address	A1	A2	A4	Address	A1	A2	A5
P-Mask	FFFFFFFF	FFFFFFFF	00000000	Mask	FFFFFFFF	FFFFFFFF	FFFFFFFF
S-Count	0001	0001	0001	S-Count	0001	0001	0001
Value	00010008	40000000					
				Third loop			
Address	A1	A2	A5	Address	A1	A2	A6
P-Mask	FFFFFFFF	FFFFFFFF	00000000	Mask	FFFFFFFF	FFFFFFFF	FFFFFFFF
S-Count	0001	0001	0001	S-Count	0001	0001	0001
Value	0001000C	20000000					
				Fourth loop			
Address	A1	A2	A6	Address	A1	A2	A7
P-Mask	FFFFFFFF	FFFFFFFF	00000000	Mask	FFFFFFFF	FFFFFFFF	FFFFFFFF
S-Count	0001	0001	0001	S-Count	0001	0001	0001
Value	00010010	10000000					

FIG. 41 (a)

Address	A1	A2	A3	
P-Mask	FFFFFFFF	FFFFFFFF	00000000	First loop
S-Count	0001	0001	0001	
Value	00010004	80000000		
	↓ diff=04	↓ diff=-4		
Address	A1	A2	A4	Second loop
P-Mask	FFFFFFFF	FFFFFFFF	00000000	
S-Count	0001	0001	0001	
Value	00010008	40000000		
	↓ diff=04	↓ diff=-2		
Address	A1	A2	A5	Third loop
P-Mask	FFFFFFFF	FFFFFFFF	00000000	
S-Count	0001	0001	0001	
Value	0001000C	20000000		
	↓ diff=04	↓ diff=-1		
Address	A1	A2	A6	Fourth loop
P-Mask	FFFFFFFF	FFFFFFFF	00000000	
S-Count	0001	0001	0001	
Value	00010010	10000000		
Assumption of distance	↓ diff=04	↓ diff=??		

FIG. 41 (b)

	Predicted value storing region		Waiting-required address storage region	
Address	A1	A2	A7	Fifth loop
Mask	FFFFFFFF	FFFFFFFF	FFFFFFFF	Predicted distance is 1 = allocation to MSP
S-Count		0000	0001	
Value	00010014	WAIT	WAIT	
Address	A1	A2	A8	Sixth loop
Mask	FFFFFFFF	FFFFFFFF	FFFFFFFF	Predicted distance is 2 = allocation to SSP#1
S-Count		0001	0001	
Value	00010018	WAIT	WAIT	
Address	A1	A2	A9	Seventh loop
Mask	FFFFFFFF	FFFFFFFF	FFFFFFFF	Predicted distance is 3 = allocation to SSP#2
S-Count		0002	0001	
Value	0001001C	WAIT	WAIT	
Address	A1	A2	A10	Eighth loop
Mask	FFFFFFFF	FFFFFFFF	FFFFFFFF	Predicted distance is 4 = allocation to SSP#3
S-Count		0003	0001	
Value	00010020	WAIT	WAIT	

Fifth loop (MSP)

FIG. 42

```

loop: (PC=1000)
  set A1 -> R1
  ld (A1=R1) -> Rx ... (00010014)
  set A2 -> R2
  ld (A2=R2) -> Ry ... (08000000)
  ld (A7=Rx-4) -> Rz ... (7800aaaa)
  add Rx+4 -> Rx ... 00010018
  st Rx -> (A1=R1) ... 00010018
  shift Ry -> Ry ... 04000000
  st Ry -> (A2=R2) ... 04000000
  add Ry+Rz -> Rz ... 7c00aaaa
  st Rz -> (A8=Rx) ... 7c00aaaa
  br loop
  
```

Sixth loop (SSP#1)

Address	A1	A2	A8
Mask	FFFFFFFF	FFFFFFFF	FFFFFFFF
S-Count		0001	0001
Value	00010018	WAIT	WAIT

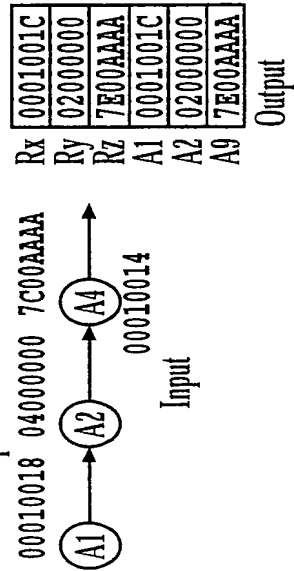
```

loop: (PC=1000)
  set A1 -> R1
  ld (A1=R1) -> Rx ... (00010018)
  set A2 -> R2
  
```

Address	A1	A2	A8
Mask	FFFFFFFF	FFFFFFFF	FFFFFFFF
S-Count		0000	0000
Value	00010018	04000000	7C00AAAA

```

  ld (A2=R2) -> Ry ... (04000000)
  ld (A8=Rx-4) -> Rz ... (7c00aaaa)
  add Rx+4 -> Rx ... 0001001c
  st Rx -> (A1=R1) ... 0001001c
  shift Ry -> Ry ... 02000000
  st Ry -> (A2=R2) ... 02000000
  add Ry+Rz -> Rz ... 7e00aaaa
  st Rz -> (A9=Rx) ... 7e00aaaa
  br loop
  
```



Seventh loop (SSP#2)

Address	A1	A2	A9
Mask	FFFFFFFF	FFFFFFFF	FFFFFFFF
S-Count		0002	0001
Value	0001001C	WAIT	WAIT

```

loop: (PC=1000)
  set A1 -> R1
  ld (A1=R1) -> Rx ... (0001001c)
  set A2 -> R2
  
```

Address	A1	A2	A9
Mask	FFFFFFFF	FFFFFFFF	FFFFFFFF
S-Count		0000	0000
Value	0001001C	02000000	7E00AAAA

```

  ld (A2=R2) -> Ry ... (02000000)
  ld (A9=Rx-4) -> Rz ... (7e00aaaa)
  add Rx+4 -> Rx ... 00010020
  st Rx -> (A1=R1) ... 00010020
  shift Ry -> Ry ... 01000000
  st Ry -> (A2=R2) ... 01000000
  add Ry+Rz -> Rz ... 7f00aaaa
  st Rz -> (A10=Rx) ... 7f00aaaa
  br loop
  
```

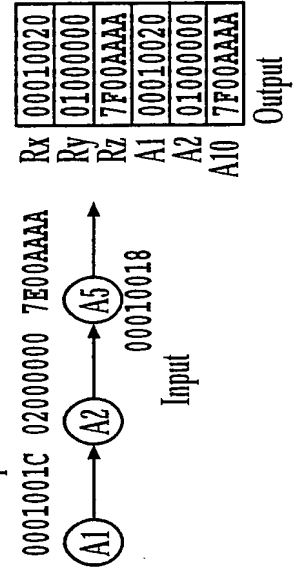


FIG. 43

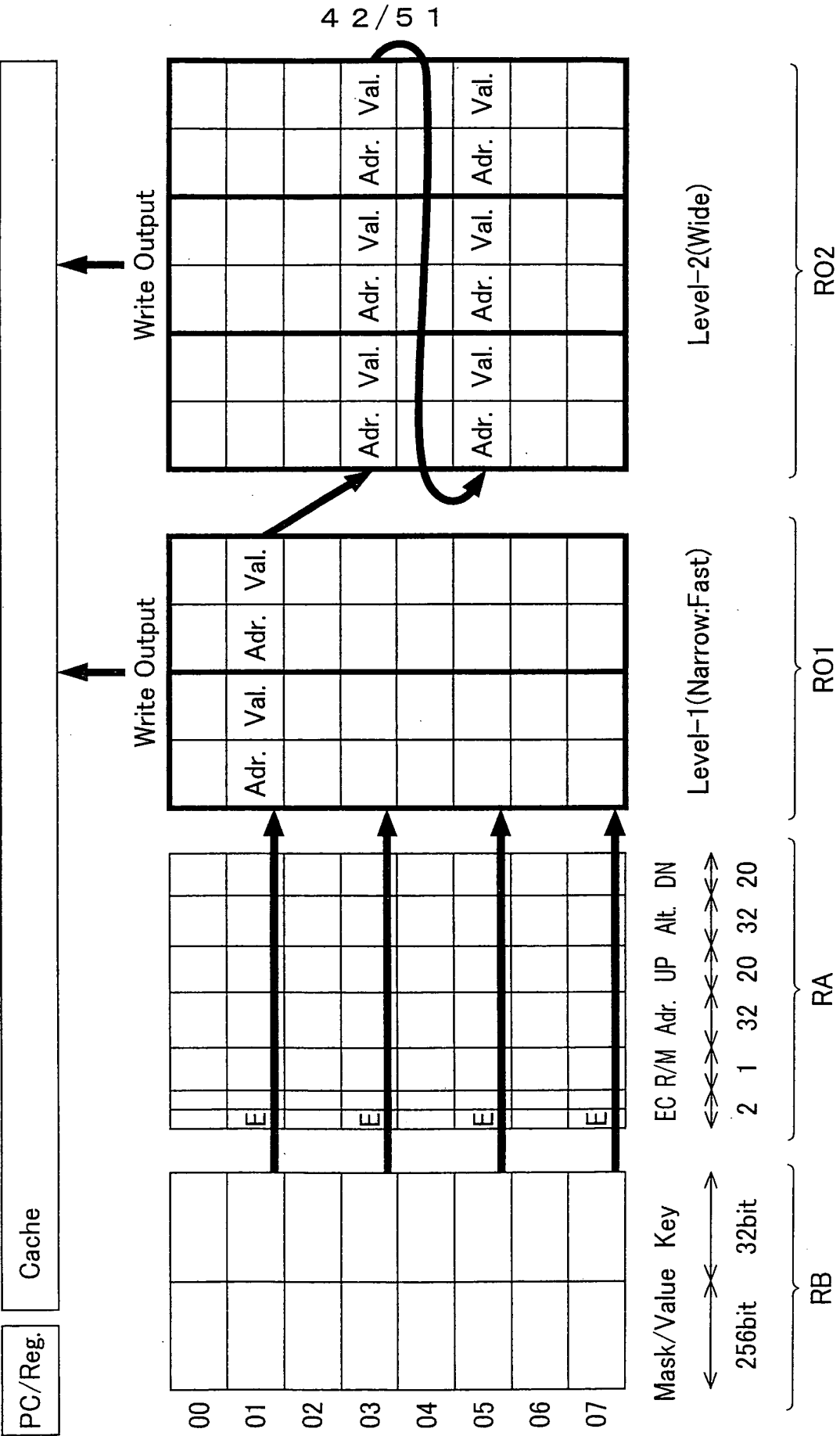
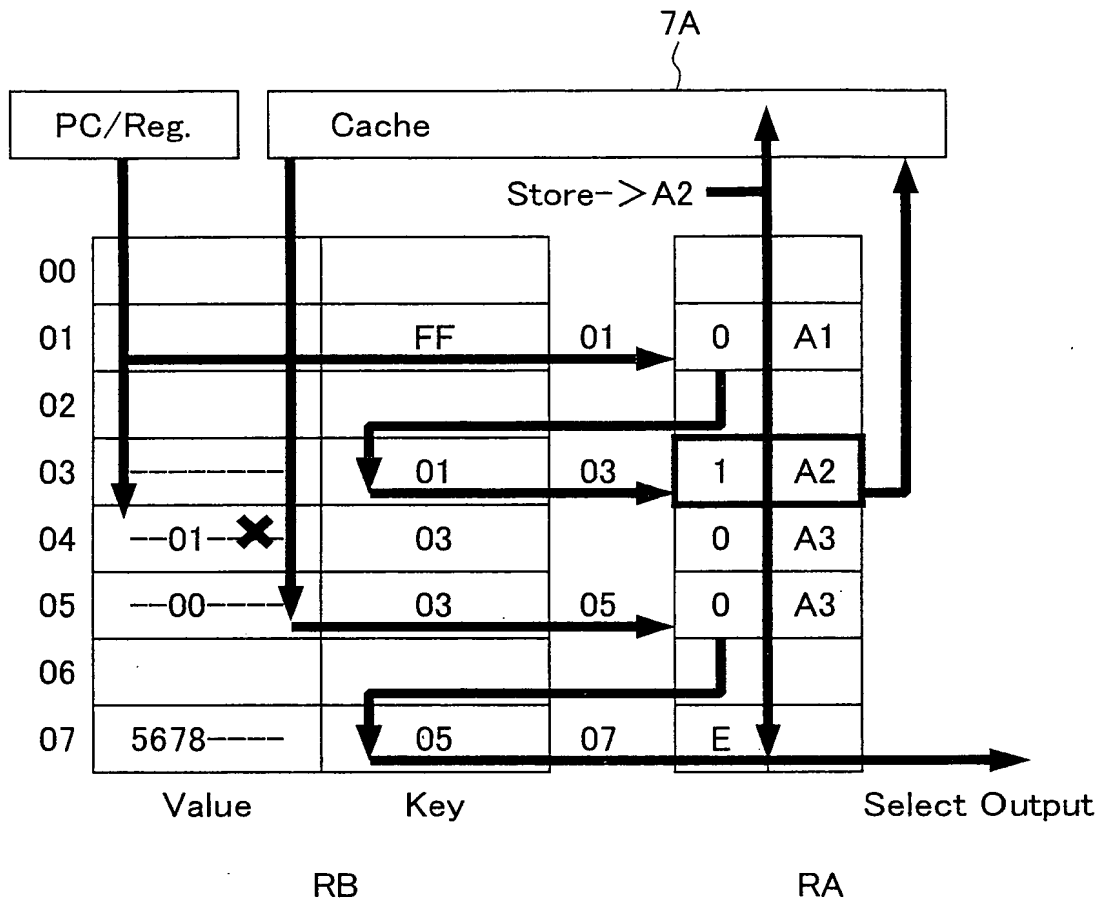


FIG. 44



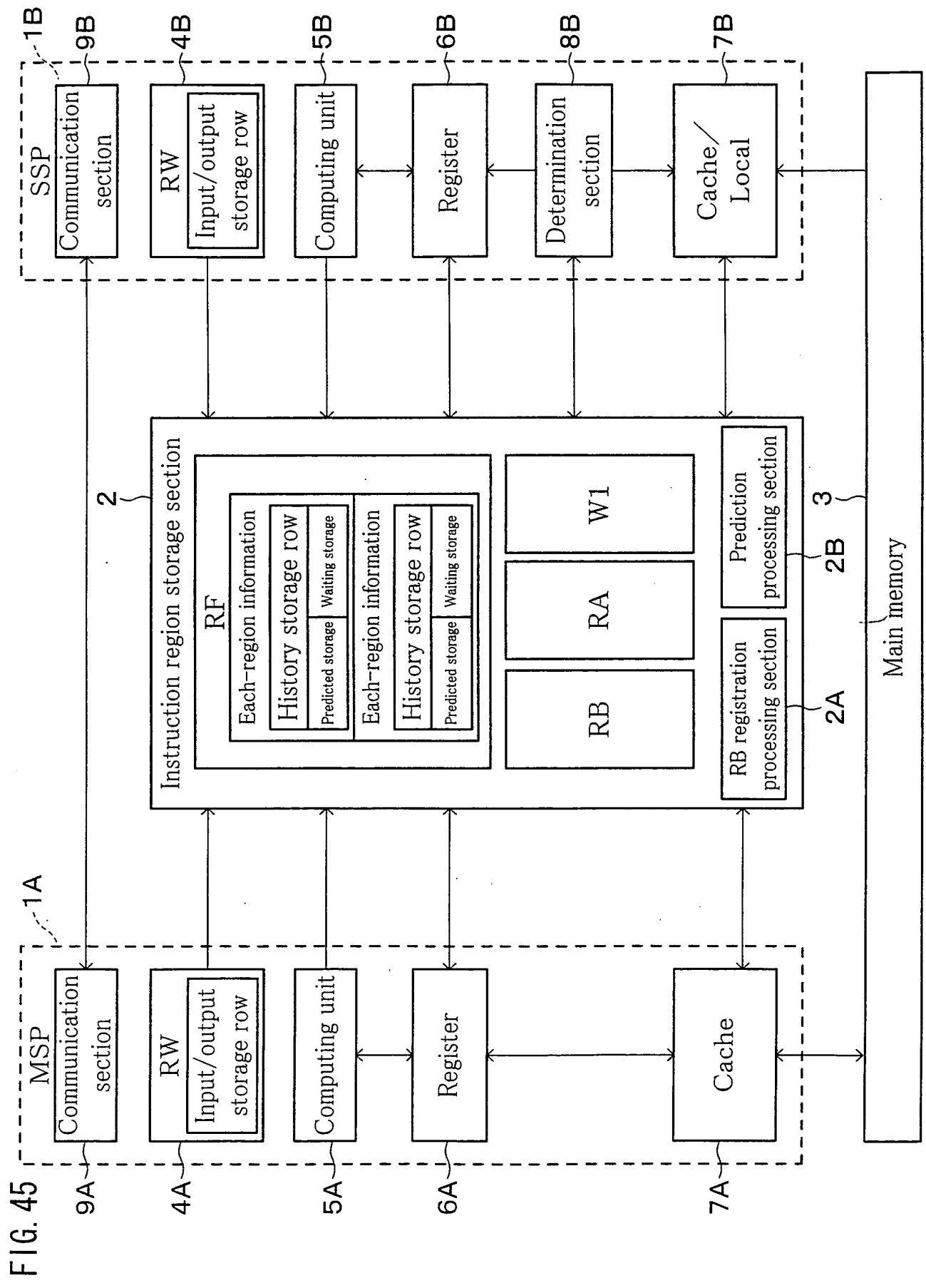


FIG. 46(a)

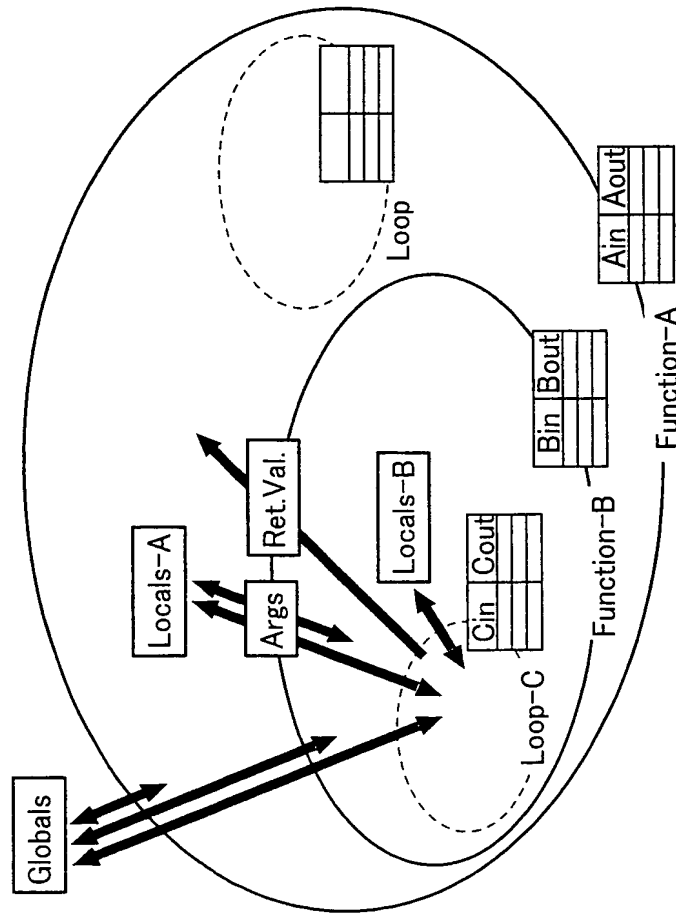


FIG. 46(b)

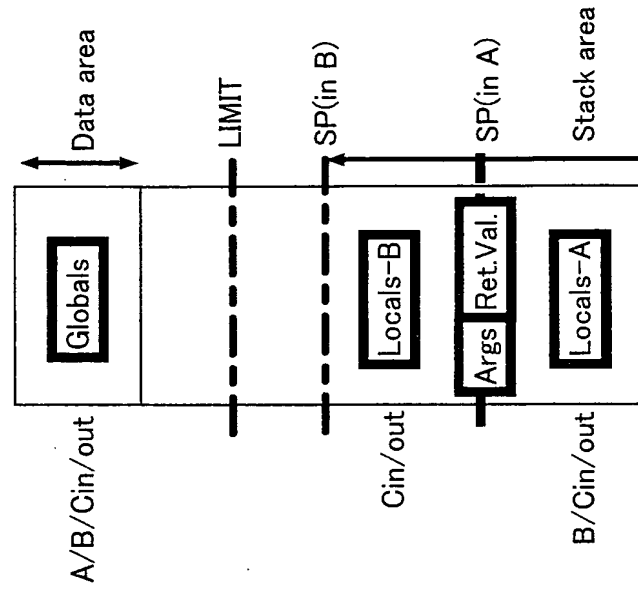
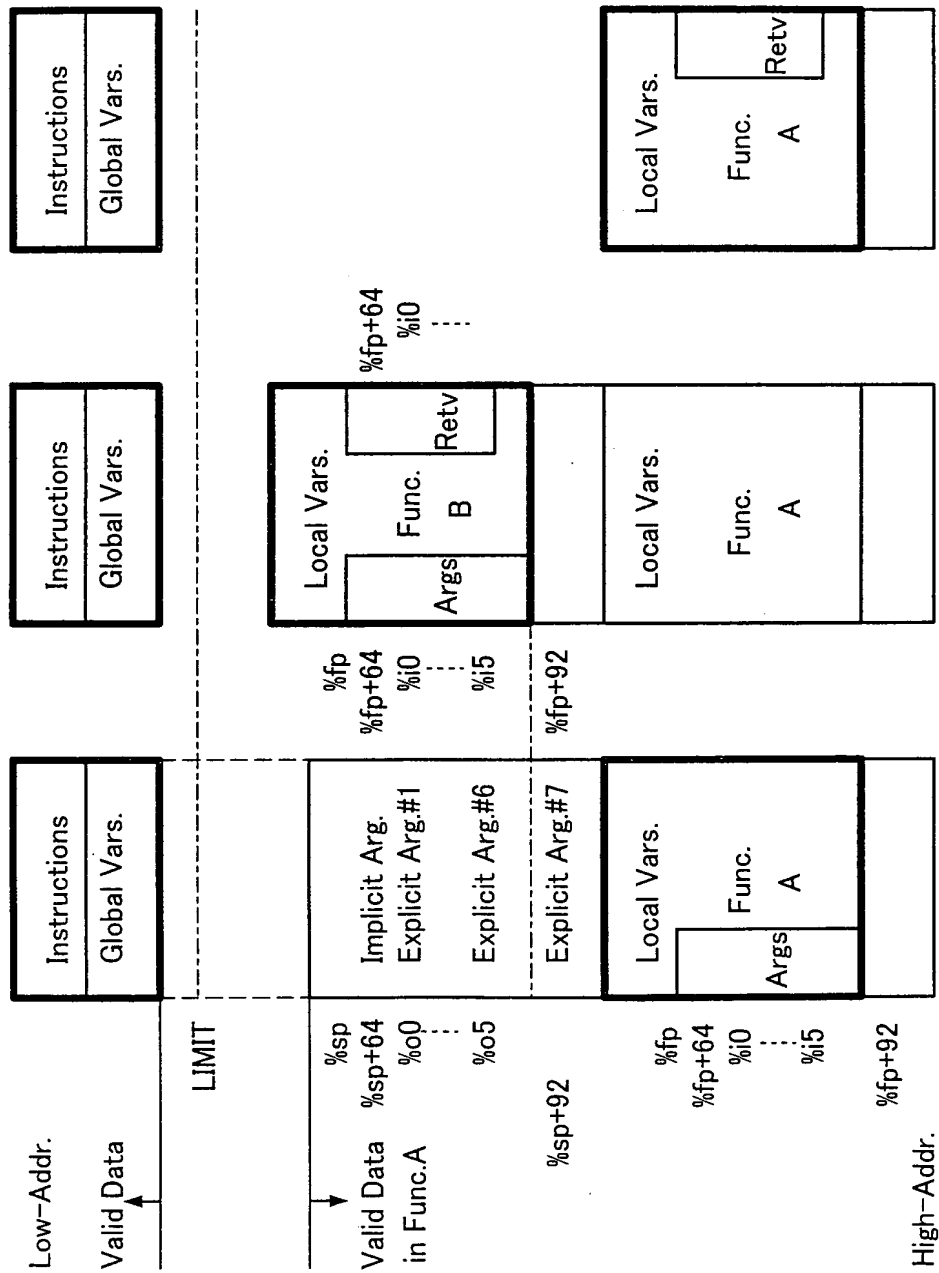


FIG. 47



(c) Return A.

(b) Call/Return B.

(a) Call A.

FIG. 48

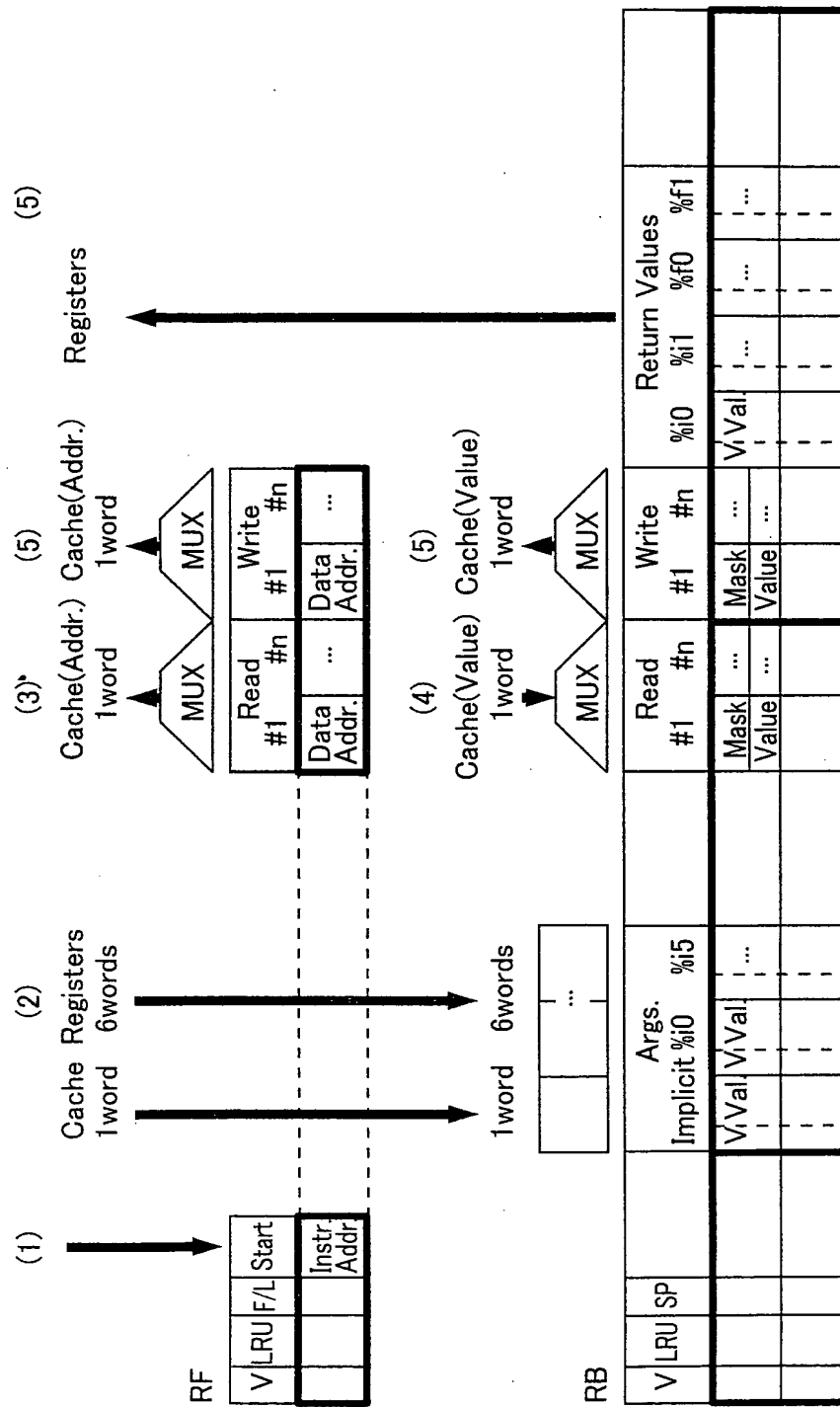


FIG. 49

PC: 1000
set A1→R0
ld (R0)→R1
set A2→R0
ldb (R0)→R2
ldb (A2+R2)→R2
set A3→R0
ldb (R0)→R3
ldb (A4=R1+R2)→R4
add R5+1→R5

FIG. 50

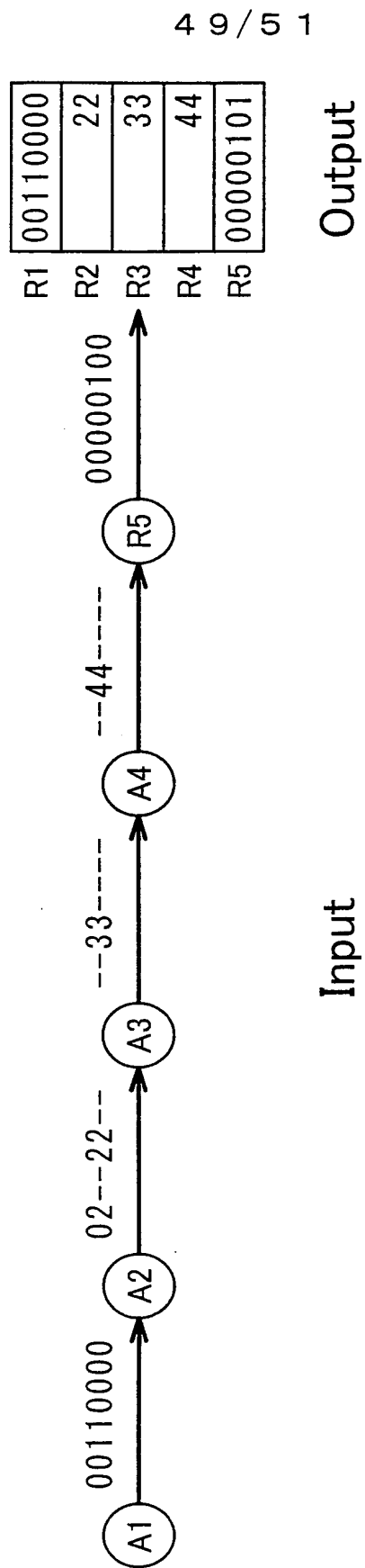


FIG. 51

Register/Memory Read						Register/Memory Write					
#1	#2	#3	#4	#5	END	#1	#2	#3	#4	#5	END
Address	A1	A2	A3	A4	R5	Address	R1	R2	R3	R4	R5
Mask	FFFFFFFF	FF00FF00	00FF0000	00FF0000	FFFFFFFF	Mask	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF	FFFFFFFF
Value	00110000	02--22--	--33----	--44----	00000100	Value	00110000	00000022	00000033	00000044	00000101

FIG. 52

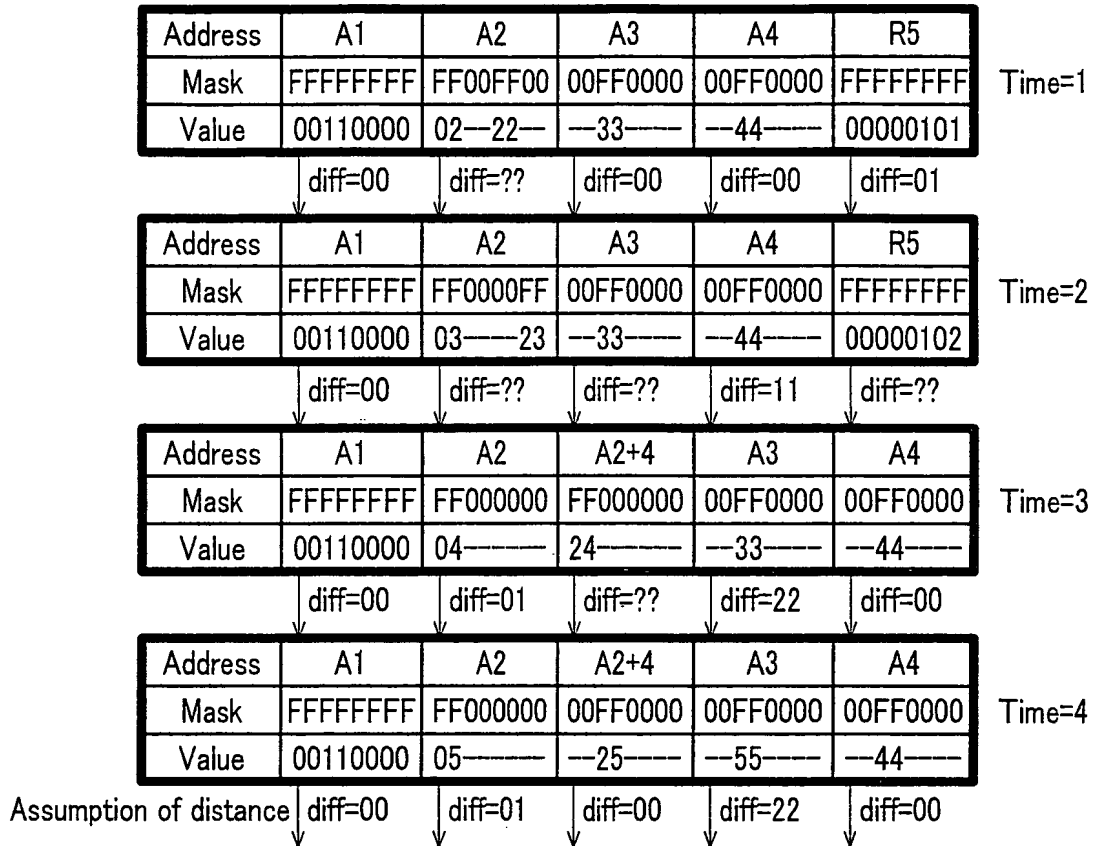


FIG. 53

Address	A1	A2	A2+4	A3	A4
Mask	FFFFFFFF	FF000000	00FF0000	00FF0000	00FF0000
Value	00110000	06—	—25—	—77—	—44—

Predicted distance=1

Address	A1	A2	A2+4	A3	A4
Mask	FFFFFFFF	FF000000	00FF0000	00FF0000	00FF0000
Value	00110000	07—	—25—	—99—	—44—

Predicted distance=2

Address	A1	A2	A2+4	A3	A4
Mask	FFFFFFFF	FF000000	00FF0000	00FF0000	00FF0000
Value	00110000	08—	—25—	—BB—	—44—

Predicted distance=3

Address	A1	A2	A2+4	A3	A4
Mask	FFFFFFFF	FF000000	00FF0000	00FF0000	00FF0000
Value	00110000	09—	—25—	—DD—	—44—

Predicted distance=4